National Semiconductor

96L02
Dual Retriggerable Resettable Monostable Multivibrator

General Description

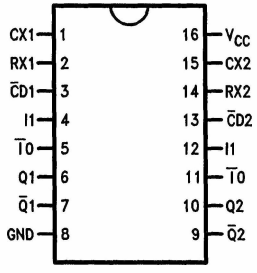
The 96L02 is a dual TTL monostable multivibrator with trigger mode selection, reset capability, rapid recovery, internally compensated reference levels and high speed capability. Output pulse duration and accuracy depend on external timing components, and are therefore under user control for each application. It is well suited for a broad variety of applications, including pulse delay generators, square wave generators, long delay timers, pulse absence detectors, frequency detectors, clock pulse generators and fixed-frequency dividers. Each input is provided with a clamp diode to limit undershoot and minimize ringing induced by fast fall times acting on system wiring impedances.

Features

- Retriggerable, 0% to 100% duty cycle
- DC level triggering, insensitive to transition times
- Leading or trailing-edge triggering
- Complementary outputs with active pull-ups
- Pulse width compensation for ΔV_{CC} and ΔT_A
- 50 ns to ∞ output pulse width range
- Optional retrigger lock-out capability
- Resettable, for interrupt operations

Connection Diagram

Dual-In-Line Package



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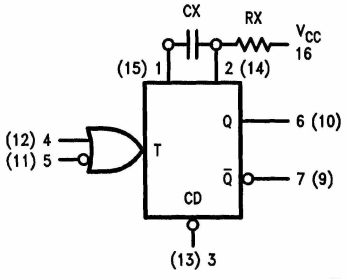
Order Number 96L02DMQB or 96L02FMQB
See NS Package Number J16A or W16A

Logic Symbol



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V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
Ī0	Trigger Input (Active Falling Edge)
I1	Trigger Input (Active Rising Edge)
$\overline{C}_D$	Direct Clear Input (Active LOW)
Q	Positive Pulse Output
$\overline{Q}$	Complementary Pulse Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Storage Temperature Range	−65°C to +150°

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Conditions	96L02 (Mil)			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.7	V
I_{OH}	High Level Output Current				0.36	mA
I_{OL}	Low Level Output Current				4.8	mA
T_A	Free Air Operating Temperature		−55		125	°C
t_w (L) t_w (H)	Minimum Input Pulse Width, I1, $\overline{I0}$	V_{CC} = 5.0V			50	ns
t_w (min)	Minimum Output Pulse Width at Q, $\overline{Q}$	V_{CC} = 5.0V, R_X = 20 kΩ C_X = 0, C_L = 15 pF	10		300	ns
t_w	Output Pulse Width, Q, $\overline{Q}$	V_{CC} = 5.0V, R_X = 39 kΩ C_X = 1000 pF	11.5		14.2	μs
R_X	Timing Resistor Range				100	kΩ

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Min, V_{IL} = Max			0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−2.0		−13.0	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			16	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

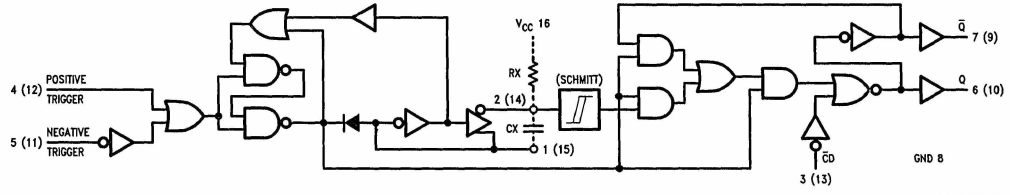
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics $V_{CC} = +5.0V, T_A = +25°C$

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay $\overline{I}0$ to Q, I1 to Q	$V_{CC} = 5.0V, R_X = 20\ k\Omega$ $C_X = 0, C_L = 15\ pF$		75	ns
t_{PHL}	Propagation Delay $\overline{I}0$ to $\overline{Q}$, I1 to $\overline{Q}$	$V_{CC} = 5.0V, R_X = 20\ k\Omega$ $C_X = 0, C_L = 15\ pF$		62	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CD}$ to $\overline{Q}$, $\overline{CD}$ to Q	$V_{CC} = 5.0V, R_X = 39\ k\Omega$ $C_X = 1000\ pF$		100	ns

Functional Block Diagram



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Operation Notes

1. TRIGGERING—can be accomplished by a positive-going transition on pin 4 (12) or a negative-going transition on pin 5 (11). Triggering begins as a signal crosses the input V_{IL}:V_{IH} threshold region; this activates an internal latch whose unbalanced cross-coupling causes it to assume a preferred state. As the latch output goes LOW it disables the gates leading to the Q output and, through an inverter, turns on the capacitor discharge transistor. The inverted signal is also fed back to the latch input to change its state and effectively end the triggering action; thus the latch and its associated feed-back perform the function of a differentiator.

   The emitters of the latch transistors return to ground through an enabling transistor which must be turned off between successive triggers in order for the latch to proceed through the proper sequence when triggering is desired. Pin 5 (11) must be HIGH in order to trigger at pin 4 (12); conversely, pin 4 (12) must be LOW in order to trigger at pin 5 (11).

2. RETRIGGERING—In a normal cycle, triggering initiates a rapid discharge of the external timing capacitor, followed by a ramp voltage run-up at pin 2 (14). The delay will time out when the ramp voltage reaches the upper trigger point of a Schmitt circuit, causing the outputs to revert to the quiescent state. If another trigger occurs before the ramp voltage reaches the Schmitt threshold, the capacitor will be discharged and the ramp will start again without having disturbed the output. The delay period can therefore be extended for an arbitrary length of time by insuring that the interval between triggers is less than the delay time, as determined by the external capacitor and resistor.

3. NON-RETRIGGERABLE OPERATION—Retriggering can be inhibited logically, by connecting pin 6 (10) back to pin 4 (12) or by connecting pin 7 (9) back to pin 5 (11). Either hook-up has the effect of keeping the latch-enabling transistor turned on during the delay period, which prevents the input latch from cycling as discussed above in the section on triggering.

4. OUTPUT PULSE WIDTH—An external resistor R_X and an external capacitor C_X are required, as shown in the functional block diagram. To minimize stray capacitance and noise pickup, R_X and C_X should be located as close as possible to the circuit. In applications which require remote trimming of the pulse width, as with a variable resistor, R_X should consist of a fixed resistor in series with the variable resistor; the fixed resistor should be located as close as possible to the circuit. The output pulse width t_w is defined as follows, where R_X is in kΩ, C_X is in pF and t_w is in ns.

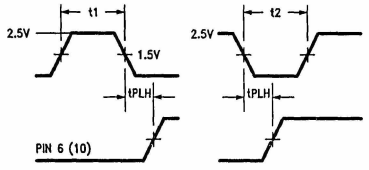
   $$t_w = 0.33\ R_X C_X\ (1 + 3/R_X) \text{ for } C_X \geq 10^3\ pF$$

   $$20\ k\Omega \leq R_X \leq 100\ k\Omega \text{ for } -55°C \text{ to } +125°C$$

   C_X may vary from 0 to any value. For pulse widths with C_X less than 10^3 pF see *Figure a.*

Operation Notes (Continued)

5. SETUP AND RELEASE TIMES—The setup times listed below are necessary to allow the latch-enabling transistor to turn off and the node voltages within the input latch to stabilize, thus insuring proper cycling of the latch when the next trigger occurs. The indicated release times (equivalent to trigger duration) allow time for the input latch to cycle and its signal to propagate.



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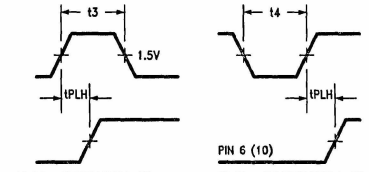
Input to Pin 5 (11)
Pin 4 (12) = L
Pin 3 (13) = H



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Input to Pin 4 (12)
Pins 5 (11) and 3 (13) = H

6. RESET OPERATION—A LOW signal on $\overline{C}_D$, pin 3 (13), will terminate an output pulse, causing Q to go LOW and $\overline{Q}$ to go HIGH. As long as $\overline{C}_D$ is held LOW, a delay period cannot be initiated nor will attempted triggering cause spikes at the outputs. A reset pulse duration, in the LOW state, of 25 ns is sufficient to insure resetting. If the reset input goes LOW at the same time that a trigger transition occurs, the reset will dominate and the outputs will not respond to the trigger. If the reset input goes HIGH coincident with a trigger transition, the circuit will respond to the trigger.

96L02 Pulse Width vs R_X and C_X

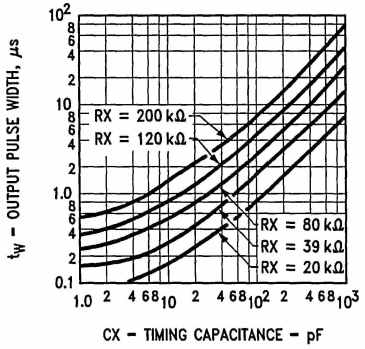

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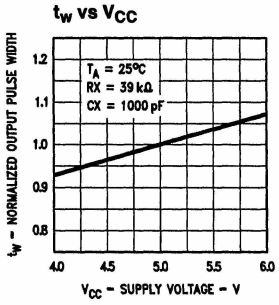
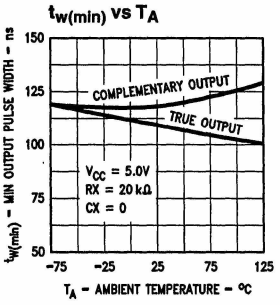
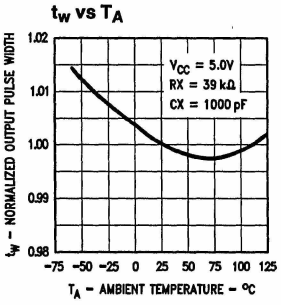
FIGURE a

Typical Characteristics







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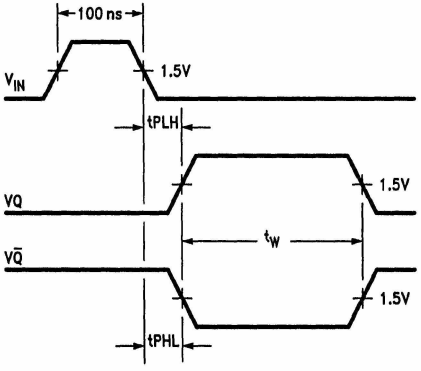

INPUT PULSE
f ≅ 25 kHz
Amp ≅ 3.0V
Width ≅ 100 ns
$t_r = t_f \leq 10$ ns

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FIGURE b