TTL MSI

DM9601/DM8601 (9601-51/9601-59) retriggerable monostable multivibrator

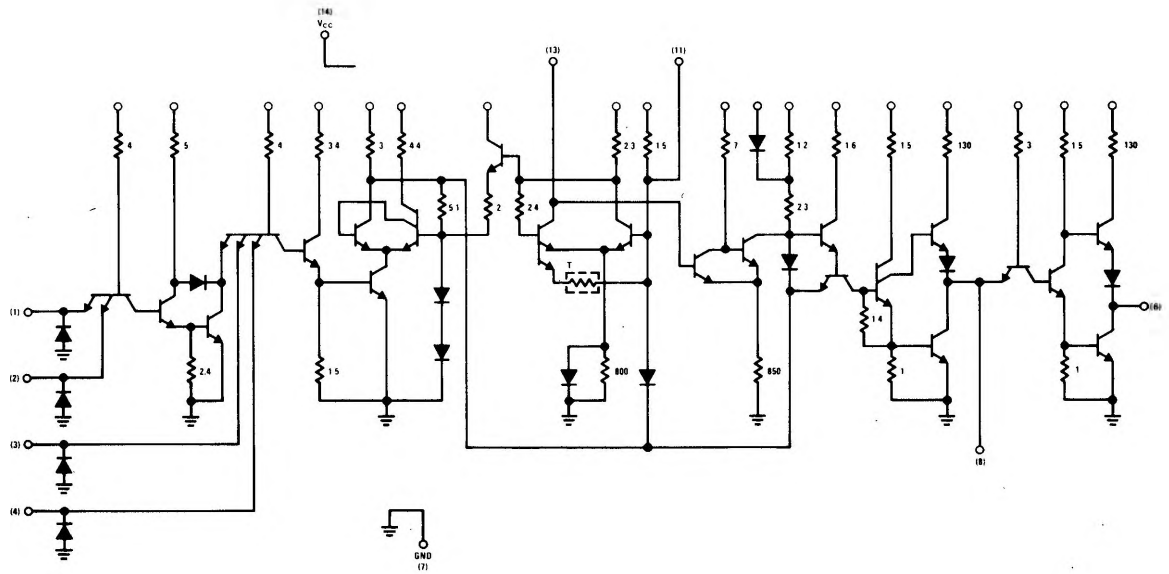
general description

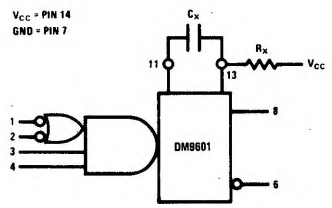
The DM9601/DM8601 is both pin-for-pin and spec-for-spec interchangeable with the 9601 one-shot. Pulse widths range from 50 ns upward depending upon the values of the external R&C used. The retriggerable feature allows for output pulse widths to be extended beyond the normal range attainable with just a resistor and capacitor.

Additional Features Include:

- Input Clamping Diodes
- Complementary DC Level Sensitive Inputs
- Flexibility of Operation—Optional Retriggering/Lockout Capability
- DTL/TTL Compatible Logic Levels
- High Speed Operation—Input Repetition Rate > 10 MHz
- Output Pulse Width Range 50 ns to ∞
- Leading or Trailing Edge Triggering
- Complementary Outputs

schematic and logic diagrams





absolute maximum ratings

Supply Voltage to Ground	−0.5V to +8.0V
Input Voltage	−0.5V to +5.5V
Voltage Applied to Outputs	−0.5V to $+V_{CC}$
Storage Temperature	−65°C to +150°C
Operating Temperature	
DM9601	−55°C to +125°C
DM8601	0°C to +75°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics DM9601(9601-51)

TABLE I

Symbol	Parameter	Limits							Units	Conditions (Note 1)
		−55°C		+25°C			+125°C			
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.4		2.4	3.3		2.4		V	V_{CC} = 4.5V I_{OH} = −0.72 mA (Note 2)
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	V	V_{CC} = 4.5V I_{OL} = 10 mA (Note 2)
V_{IH}	Input High Voltage	2.0		1.7			1.4		V	V_{CC} = 4.5V
V_{IL}	Input Low Voltage		0.85			0.90		0.85	V	V_{CC} = 5.5V (Note 3)
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5V V_F = 0.4V
I_R	Input Leakage Current				15	60		60	μA	V_{CC} = 5.5V V_R = 4.5V
I_{SC}	Short Circuit Current			−10		−40				V_{CC} = 5.0V V_{OUT} = 0V (Note 2)
I_{PD}	Quiescent Power Supply Drain		25			25		25	mA	V_{CC} = 5.5V
t_{pd-}	Negative Trigger Input to True Output				25	40			ns	V_{CC} = 5.0V R_X = 5.0 KΩ
t_{pd-}	Negative Trigger Input to Complement Output				25	40			ns	C_X = 0 C_L = 15 pF
$t_{pw(min)}$	Minimum True Output Pulse Width				45	65			ns	
Δt_{pw}	Pulse Width Variation			3.08	3.42	3.76			μs	V_{CC} = 5.0V R_X = 10 KΩ, C_X = 1,000 pF
C_{stray}	Maximum Allowable Wiring Capacitance (Pin 13)		50			50		50	pF	Pin 13 to GND
R_X	External Timing Resistor	5.0	25	5.0		25	5.0	25	kΩ	

Note 1: Unless otherwise specified, R_X = 10 KΩ between Pin 13 and V_{CC} on all tests.

Note 2: Ground Pin 11 for V_{OL} test on Pin 6, V_{OH} test on Pin 8 and I_{SC} test on Pin 8. Open Pin 11 for V_{OL} test on Pin 8, V_{OH} test on Pin 6 and I_{SC} test on Pin 6.

Note 3: Pulse test to determine V_{IH} and V_{IL} (Min PW = 40 ns).

electrical characteristics DM8601(9601-59)

TABLE II

Symbol	Parameter	Limits							Units	Conditions (Note 1)
		0°C		+25°C			+75°C			
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.4		2.4	3.4		2.4		V	V_{CC} = 4.75V I_{OH} = -0.96 mA (Note 2)
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	V	V_{CC} = 4.75V I_{OL} = 12.8 mA (Note 2)
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	V_{CC} = 4.75V
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	V_{CC} = 5.25V (Note 3)
I_F	Input Load Current		-1.6		-1.0	-1.6		-1.6	mA	V_{CC} = 5.25V V_F = 0.45V
I_R	Input Leakage Current				15	60		60	μA	V_{CC} = 5.25V V_R = 4.5V
I_{SC}	Short Circuit Current			-10		-40			mA	V_{CC} = 5.0V V_{OUT} = 0V (Note 2)
I_{PD}	Quiescent Power Supply Drain		25			25		25	mA	V_{CC} = 5.25V GND Pins 1 & 2
t_{pd+}	Negative Trigger Input to True Output				25	40			ns	V_{CC} = 5.0V R_X = 5.0 KΩ
t_{pd-}	Negative Trigger Input to Complement Output				25	40			ns	C_X = 0 C_L = 15 pF
$L_{pw(min)}$	Minimum True Output Pulse Width				45	65			ns	
Δt_{pw}	Pulse Width Variation			3.08	3.42	3.76			μs	V_{CC} = 5.0V R_X = 10 KΩ, C_X = 1,000 pF
C_{stray}	Maximum Allowable Wiring Capacitance (Pin 13)		50			50		50	pF	Pin 13 to GND
R_X	External Timing Resistor	5.0	50	5.0		50	5.0	50	kΩ	

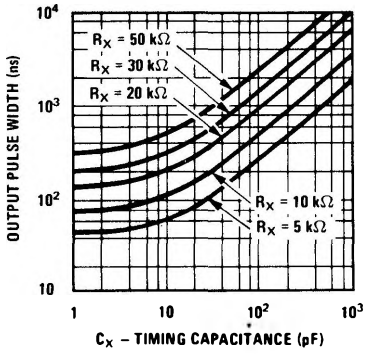
Note 1: Unless otherwise specified, R_X = 10 KΩ between Pin 13 and V_{CC} on all tests.

Note 2: Ground Pin 11 for V_{OL} test on Pin 6, V_{OH} test on Pin 8 and I_{SC} test on Pin 8.
Open Pin 11 for V_{OL} test on Pin 8, V_{OH} test on Pin 6 and I_{SC} test on Pin 6.

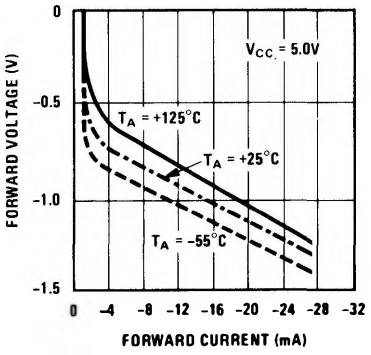
Note 3: Pulse test to determine V_{IH} and V_{IL} (Min PW = 40 ns).

typical performance characteristics

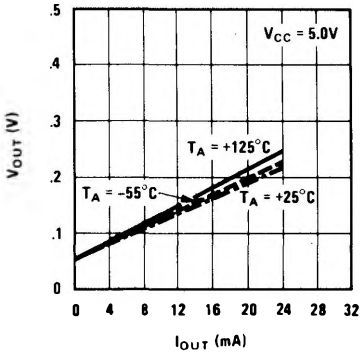
Output Pulse Width vs R_X and C_X for $C_X < 10^3$ pF



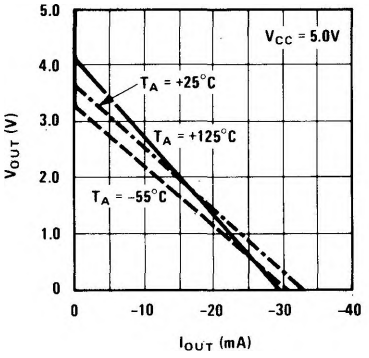
Input Clamp Diode Characteristics



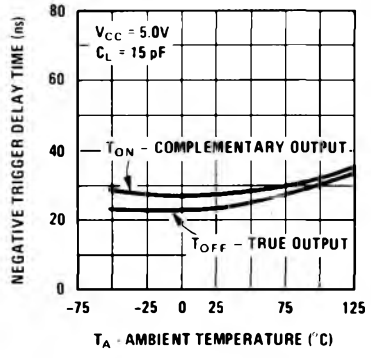
Logical "0" Output Voltage vs Sink Current



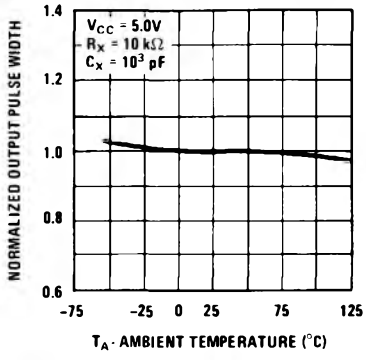
Logical "1" Output Voltage vs Source Current



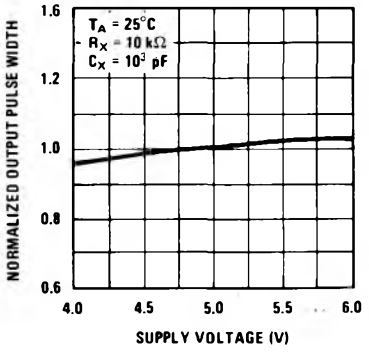
Negative Trigger Delay Time vs Ambient Temperature



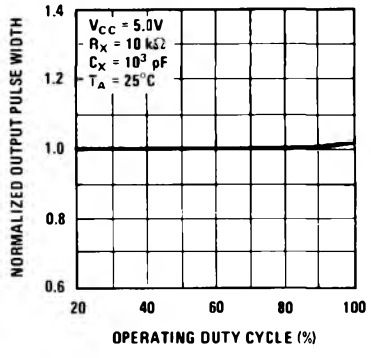
Normalized Output Pulse Width vs Ambient Temperature



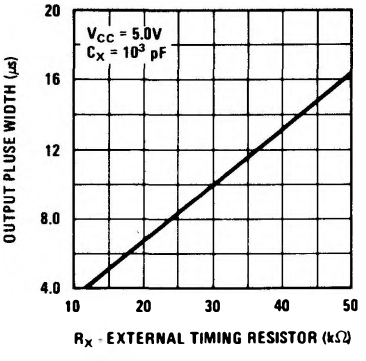
Normalized Output Pulse Width vs Supply Current



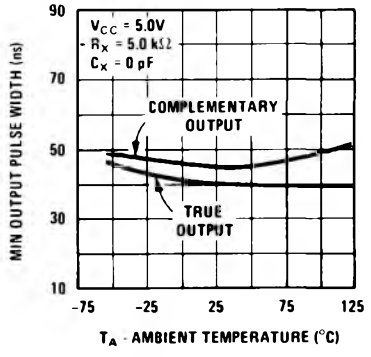
Normalized Output Pulse Width vs Operating Duty Cycle



Pulse Width vs Timing Resistance



Output Pulse Width vs Ambient Temperature



operating rules

1. An external resistor R_X and an external capacitor C_X are required for operation. The value of R_X can vary between the limits shown on tables I and II. The value of C_X is optional and may be adjusted to achieve the required output pulse width.
2. Output pulse width t_{pw} may be calculated as follows:

   $$t_{pw} = 0.32\ R_X C_X \left[1 + \frac{0.7}{R_X}\right] \text{ (for } C_X \geq 10^3 \text{ pF)}$$

   R_X in KΩ, C_X in pF and t_{pw} in ns

   For $C_X < 10^3$ pF, see curve.
3. R_X and C_X must be kept as close as possible to the circuit in order to minimize stray capacitance and noise pickup. If remote trimming is required, R_X may be split up such that at least $R_{X(MIN)}$ must be as close as possible to the circuit and the remote portion of the trimming resistor $R < R_{X(MAX)} - R_X$
4. Set-up time(t_1) for input trigger pulse >40 ns. (See Figure 1)

   Release time(t_2) for input trigger pulse >40 ns. (See Figure 2)
5. Retrigger pulse width (see Figure 3) is calculated as follows:

   $$t_w = t_{pw} + t_{pd+} = 0.32\ R_X C_X \left[1 + \frac{0.7}{R_X}\right] + t_{pd+}$$

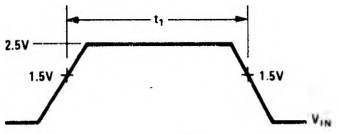


Figure 1

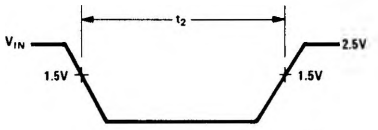


Figure 2

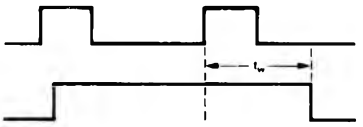
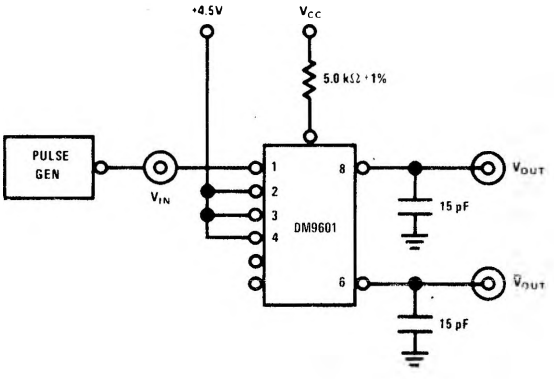
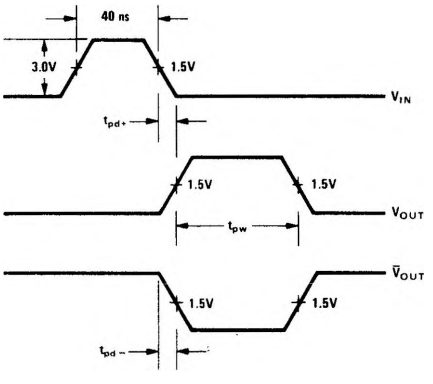


Figure 3

ac test circuit



switching time waveform



NOTE: Capacitance includes Jig and Probe