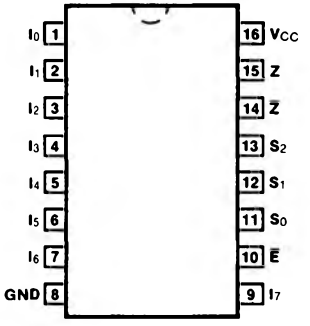
9312
93L12
93S12

8-INPUT MULTIPLEXER

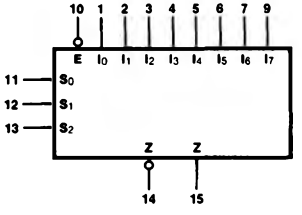
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '12 is a monolithic, high speed, 8-input digital multiplexer circuit. It provides, in one package, the ability to select one bit of data from up to eight sources. The '12 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9312PC, 93L12PC 93S12PC		9B
Ceramic DIP (D)	A	9312DC, 93L12DC 93S12DC	9312DM, 93L12DM 93S12DM	6B
Flatpak (F)	A	9312FC, 93L12FC 93S12FC	9312FM, 93L12FM 93S12FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93S (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
$S_0 - S_2$	Select Inputs	1.0/1.0	1.25/1.25	0.5/0.25
$\bar{E}$	Enable Input (Active LOW)	1.0/1.0	1.25/1.25	0.5/0.25
$I_0 - I_7$	Multiplexer Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Z	Multiplexer Output	20/10	25/12.5	10/5.0 (3.0)
$\bar{Z}$	Complementary Multiplexer Output	20/10	25/12.5	10/5.0 (3.0)

FUNCTIONAL DESCRIPTION — The '12 is a logical implementation of a single pole, eight position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Enable input ($\overline{E}$) is active LOW. When it is not activated the negation output is HIGH and the assertion output is LOW, regardless of all other inputs. The logic function provided at the output is:

$$Z = E \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2).$$

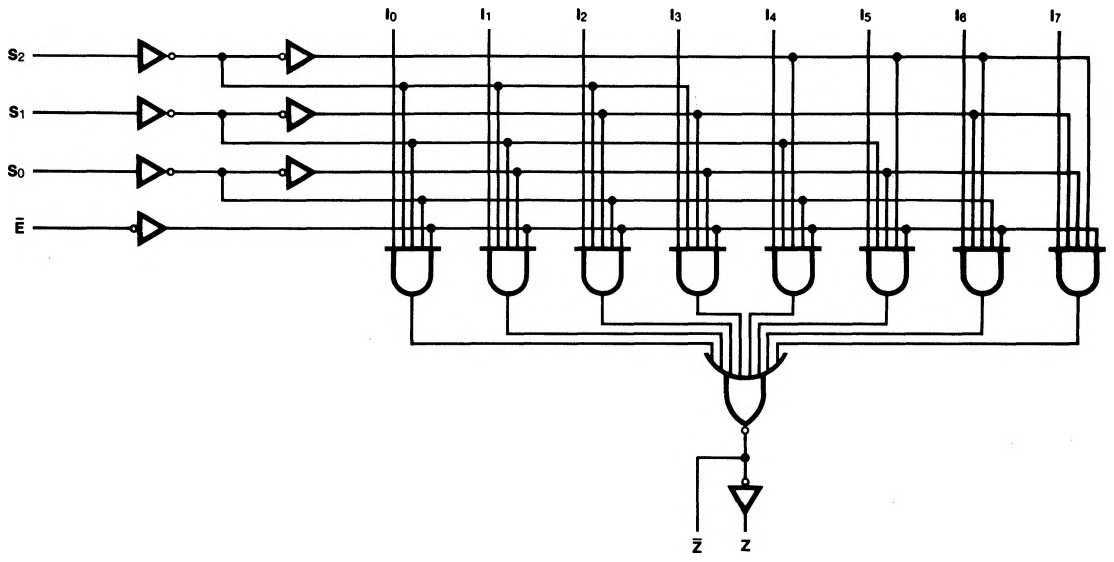
The '12 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the '12 can provide any logic function of four variables and its negation. Thus any number of random logic elements used to generate unusual truth tables can be replaced by one '12.

TRUTH TABLE

INPUTS												OUTPUTS	
$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93S		93L		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
I_{CC}	Power Supply Current		44		62		13.3	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF		93S C_L = 15 pF		93L C_L = 15 pF		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay		34		17		60	ns	Figs. 3-1, 3-5
t_{PHL}	S_0 to Z		34		18		75		
t_{PLH}	Propagation Delay		24		16		45	ns	Figs. 3-1, 3-4
t_{PHL}	S_0 to $\overline{Z}$		26		15		65		
t_{PLH}	Propagation Delay		30		13		50	ns	Figs. 3-1, 3-4
t_{PHL}	$\overline{E}$ to Z		30		16		70		
t_{PLH}	Propagation Delay		20		14		35	ns	Figs. 3-1, 3-5
t_{PHL}	$\overline{E}$ to $\overline{Z}$		23		11		60		
t_{PLH}	Propagation Delay		24		12		60	ns	Figs. 3-1, 3-5
t_{PHL}	I_n to Z		24		12		55		
t_{PLH}	Propagation Delay		14		8.0		45	ns	Figs. 3-1, 3-4
t_{PHL}	I_n to $\overline{Z}$		16		9.0		45		