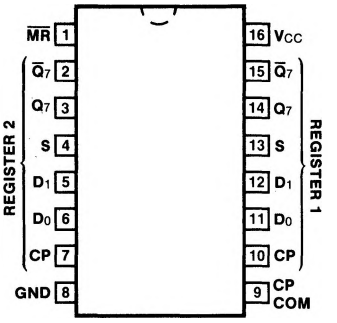
9328
93L28
DUAL 8-BIT SHIFT REGISTER

DESCRIPTION — The '28 is a high speed serial storage element providing 16 bits of storage in the form of two 8-bit registers. The multifunctional capability of this device is provided by several features: 1) additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources; 2) the clock of each register may be provided separately or together; 3) both the true and complementary outputs are provided from each 8-bit register, and both registers may be master cleared from a common input.

- **2-INPUT MULTIPLEXER PROVIDED AT DATA INPUT OF EACH REGISTER**
- **GATED CLOCK INPUT CIRCUITRY**
- **BOTH TRUE AND COMPLEMENTARY OUTPUTS PROVIDED FROM LAST BIT OF EACH REGISTER**
- **ASYNCHRONOUS MASTER RESET COMMON TO BOTH REGISTERS**

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9328PC, 93L28PC		9B
Ceramic DIP (D)	A	9328DC, 93L28DC	9328DM, 93L28DM	6B
Flatpak (F)	A	9328FC, 93L28FC	9328FM, 93L28FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

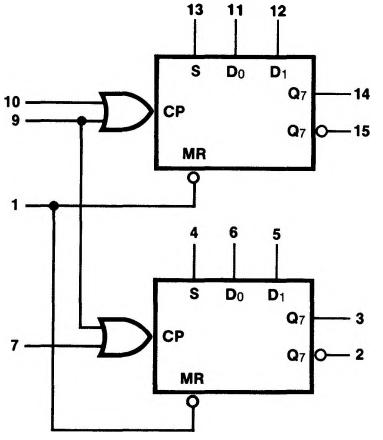
PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
S	Data Select Input	2.0/2.0	1.0/0.5
D_0, D_1	Data Inputs	1.0/1.0	0.5/0.25
CP	Clock Pulse Input (Active HIGH)		
	Common (Pin 9)	3.0/3.0	1.5/0.75
	Separate (Pins 7 and 10)	1.5/1.5	0.75/0.375
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0	0.5/0.25
Q_7	Last Stage Output	20/10	10/5.0 (3.0)
$\bar{Q}_7$	Complementary Output	20/10	10/5.0 (3.0)

FUNCTIONAL DESCRIPTION — The two 8-bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 and 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master/slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR gate are LOW, the slave latches are steady, but data can enter the master latches via the R and S input. During the first LOW-to-HIGH transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain HIGH. During the HIGH-to-LOW transition of the last remaining HIGH clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state. The data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic HIGH signal. Each 8-bit shift register has a 2-input multiplexer in front of the serial data input. The two data inputs D_0 and D_1 are controlled by the data select input (S) following the Boolean expression:

Serial data in: $S_D = SD_0 + SD_1$

An asynchronous master reset is provided which, when activated by a LOW logic level, will clear all 16 stages independently of any other input signal.

LOGIC SYMBOL



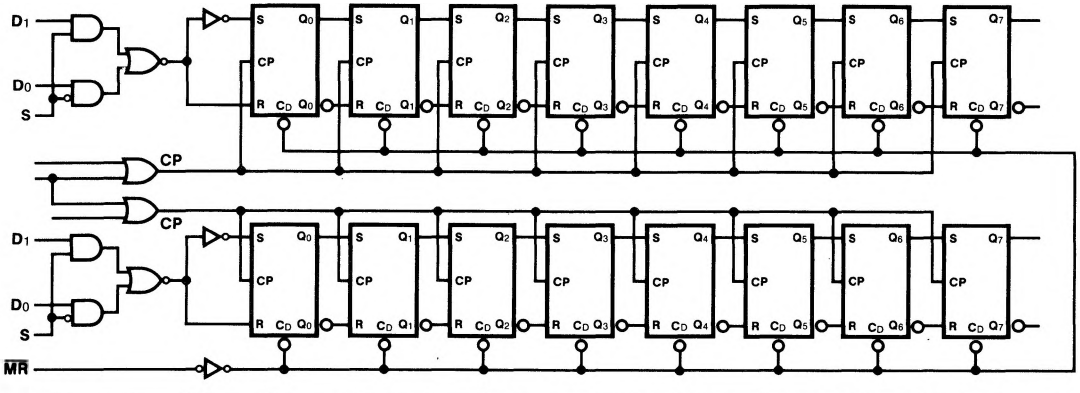
V_{CC} = Pin 16
GND = Pin 8

SHIFT SELECT TABLE

INPUTS			OUTPUT
S	D_0	D_1	Q_7 (t_n + 8)
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
n + 8 = Indicates state after eight clock pulse

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		77		25.3	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C_L = 15 pF R_L = 400 Ω		C_L = 15 pF			
		Min	Max	Min	Max		
f_{max}	Maximum Shift Right Frequency	20		5.0		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_7 or $\overline{Q}_7$		20 35		45 80	ns	Figs. 3-1, 3-8
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_7		50		110	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		MIn	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to CP	20 20		30 30		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to CP	0 0		0 0		ns	
t_w (H) t_w (L)	Clock Pulse Width HIGH or LOW	25 25		55 55		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width with CP HIGH	30		60		ns	Fig. 3-16
t_w (L)	$\overline{MR}$ Pulse Width with CP LOW	40		70		ns	
t_{rec}	Recovery Time $\overline{MR}$ to CP	33				ns	Fig. 3-16