National Semiconductor

93L14 Quad Latch

General Description

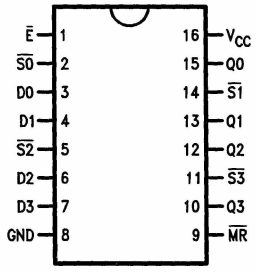
The 93L14 is a multifunctional 4-bit latch designed for general purpose storage applications in high speed digital systems. All outputs have active pull-up circuitry to provide high capacitance drive and to provide low impedance in both logic states for good noise immunity.

Features

- Can be used as single input D latches or set/reset latches
- Active low enable gate input
- Overriding master reset

Connection Diagram

Dual-In-Line Package



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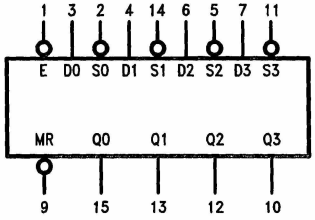
Order Number 93L14DMQB or 93L14FMQB
See NS Package Number J16A or W16A

Logic Symbol



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V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
$\overline{E}$	Enable Input (Active LOW)
D0–D3	Data Inputs
$\overline{S}$0–$\overline{S}$3	Set Inputs (Active LOW)
$\overline{MR}$	Master Reset Input (Active LOW)
Q0–Q3	Latch Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L14 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Voltage			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to $\overline{E}$	10 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to $\overline{E}$	0 10			ns
t_s (H)	Setup Time HIGH, D_n to $\overline{S}_n$	15			ns
t_h (L)	Hold Time LOW, D_n to $\overline{S}_n$	5			ns
t_w (L)	$\overline{E}$ Pulse Width LOW	30			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	25			ns
t_{rec}	Recovery Time, $\overline{MR}$ to $\overline{E}$	5			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Inputs			20	μA
			D_n			30	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	Inputs			−400	μA
			D_n			−600	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				16.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n		45 36	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		30 30	ns
t_{PLH}	Propagation Delay, $\overline{MR}$ to Q_n		30	ns
t_{PHL}	Propagation Delay, $\overline{S}_n$ to Q_n		33	ns

Functional Description

The 93L14 consists of four latches with a common active LOW Enable input and active LOW Master Reset input. When the Enable goes HIGH, data present in the latches is stored and the state of the latch is no longer affected by the $\overline{S}_n$ and D_n inputs. The Master Reset when activated overrides all other input conditions forcing all latch outputs LOW. Each of the four latches can be operated in one of two modes:

D-TYPE-LATCH—For D-type operation the $\overline{S}$ input of a latch is held LOW. While the common Enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the Enable goes HIGH.

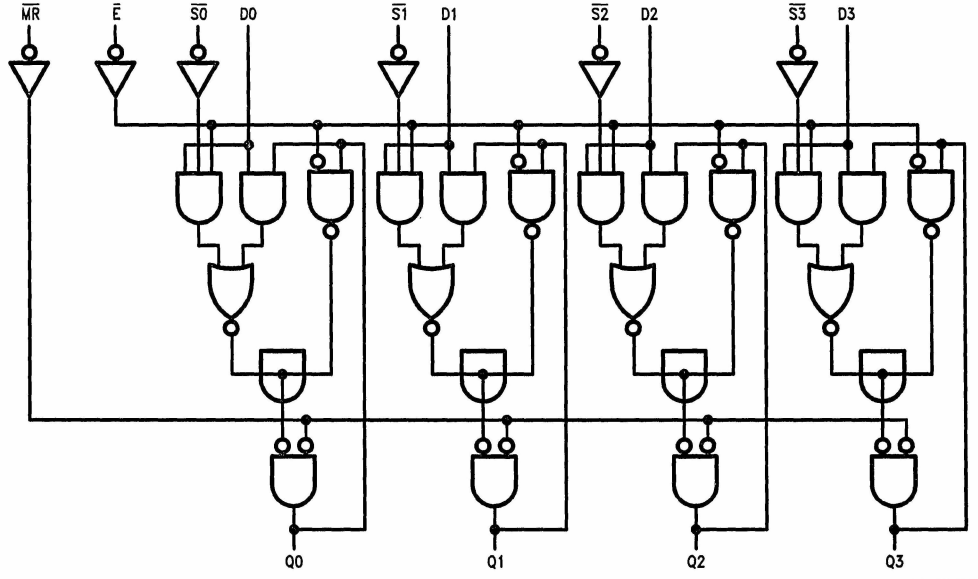
SET/RESET LATCH—During set/reset operation when the common Enable is LOW a latch is reset by a LOW on the D input, and can be set by a LOW on the $\overline{S}$ input if the D input is HIGH. If both $\overline{S}$ and D inputs are LOW, the D input will dominate and the latch wil be reset. When the Enable goes HIGH, the latch remains in the last state prior to disablement. The two modes of latch operation are shown in the Truth Table.

Truth Table

$\overline{MR}$	$\overline{E}$	D	$\overline{S}$	Q_n	Operation
H	L	L	L	L	D Mode
H	L	H	L	L	
H	H	X	X	Q_{n-1}	
H	L	L	L	L	R/S Mode
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{n-1}	
H	H	X	X	Q_{n-1}	
L	X	X	X	L	RESET

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Q_{n-1} = Previous Output State
Q_n = Present Output State

Logic Diagram



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