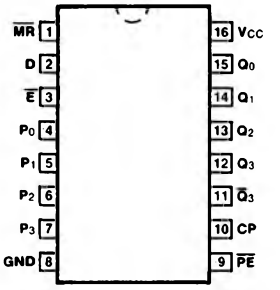
# 93H72

## HIGH SPEED 4-BIT SHIFT REGISTER

(With Enable)

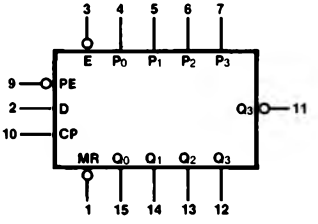
**CONNECTION DIAGRAM**
PINOUT A




**DESCRIPTION** — The '72 high speed 4-bit shift register is a multifunctional sequential logic block which is useful in a wide variety of register applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial and parallel-parallel data transfers. The '72 has three synchronous modes of operation: shift, parallel load and hold (do nothing). The hold capability permits information storage in the register independent of the clock.

- **60 MHz TYPICAL SHIFT FREQUENCY**
- **SYNCHRONOUS PARALLEL DATA ENTRY**
- **DATA HOLD (DO NOTHING) INDEPENDENT OF CLOCK**
- **FULLY SYNCHRONOUS, EDGE-TRIGGERED**
- **ASYNCHRONOUS MASTER RESET**

**LOGIC SYMBOL**




VCC = Pin 16
GND = Pin 8

**ORDERING CODE:** See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE<br>VCC = +5.0 V ±5%,<br>TA = 0°C to +70°C | MILITARY GRADE<br>VCC = +5.0 V ±10%,<br>TA = -55°C to +125°C | PKG TYPE |
|---|---|---|---|---|
| Plastic DIP (P) | A | 93H72PC | | 9B |
| Ceramic DIP (D) | A | 93H72DC | 93H72DM | 6B |
| Flatpak (F) | A | 93H72FC | 93H72FM | 4L |

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PIN NAMES | DESCRIPTION | 93H (U.L.)<br>HIGH/LOW |
|---|---|---|
| $\overline{E}$ | Enable Input (Active LOW) | 2.0/2.0 |
| $\overline{PE}$ | Parallel Enable Input (Active LOW) | 1.0/1.0 |
| $P_0 - P_3$ | Parallel Data Inputs | 1.0/1.0 |
| CP | Clock Pulse Input | 2.0/2.0 |
| $\overline{MR}$ | Master Reset Input (Active LOW) | 1.0/1.0 |
| D | Serial Data Input | 1.0/1.0 |
| $Q_0 - Q_3$ | Parallel Outputs | 20/10 |
| $\overline{Q}_3$ | Last Stage Complementary Output | 20/10 |

**FUNCTIONAL DESCRIPTION** — The '72 is a 4-bit shift register with three modes of operation: shift, parallel load and hold (do nothing). The register is fully synchronous with any output change occuring after the rising clock edge. The '72 features edge-triggered type characteristics on all inputs (except $\overline{MR}$) which means there are no restrictions on the activity of these inputs ($\overline{PE}$, $\overline{E}$, $P_0 - P_3$, D) for logic operation except for the setup requirements prior to the LOW-to-HIGH clock transition.

The mode of operation of the '72 is determined by the two inputs, Parallel Enable ($\overline{PE}$) and Enable ($\overline{E}$) as shown in Table 1. The active LOW Enable when HIGH, places the register in the hold mode with the register flip-flops retaining their information. When the Enable is activated (LOW) the Parallel Enable ($\overline{PE}$) determines whether the register operates in a shift or parallel data entry mode.

When the Enable is LOW and the Parallel Enable input is LOW the parallel inputs are selected and will determine the next condition of the register synchronously with the clock as shown in Table II. In this mode the element appears as four common clocked D flip-flops. With $\overline{E}$ LOW and the $\overline{PE}$ input HIGH the device acts as a 4-bit shift register with serial data entry through the D input shown in Table III. In both cases the next state of the flip-flops occurs after the LOW-to-HIGH transition of the clock input.

The asynchronous active LOW Master Reset overrides all inputs and clears the register forcing outputs $Q_0 - Q_3$ LOW and $\overline{Q}_3$ HIGH. To provide for left shift operation, $P_3$ is used as the serial data input and $Q_0$ is the serial data output. The other outputs are tied back to the previous parallel inputs, with $Q_3$ tied to $P_2$, $Q_2$ tied to $P_1$ and $Q_1$ tied to $P_0$.

**LOGIC DIAGRAM**

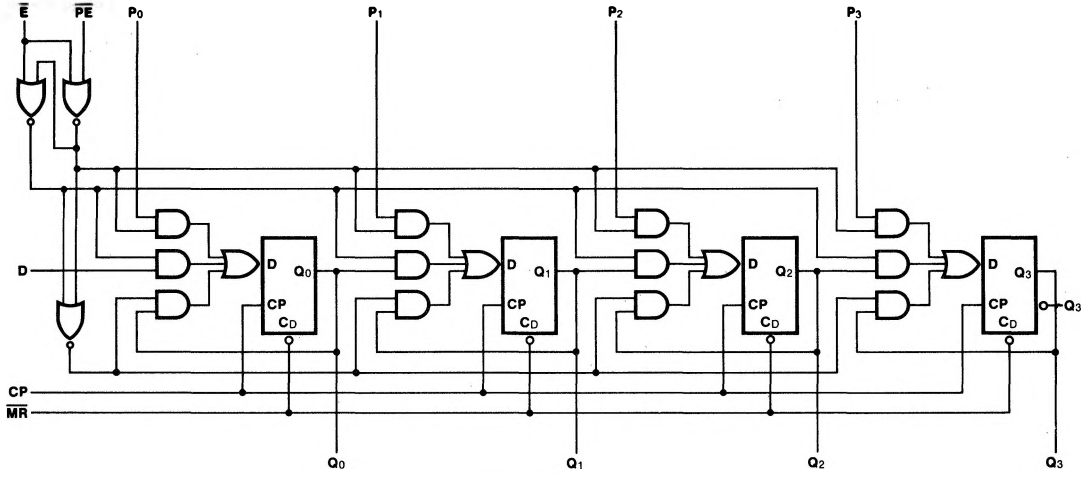



**TABLE I. MODE SELECT TABLE**

| MODE | | $\overline{MR}$ | $\overline{E}$ | $\overline{PE}$ | $P_0$ | $P_1$ | $P_2$ | $P_3$ | D |
|---|---|---|---|---|---|---|---|---|---|
| Synchronous | Parallel Load | H | L | L | Parallel Data Entry | | | | X |
| | Serial Shift | H | L | H | X | X | X | X | Serial Data Entry |
| | Hold | H | H | L | X | X | X | X | X |
| | Hold | H | H | H | X | X | X | X | X |
| Asynchronous | Reset | L | X | X | All Outputs Set LOW ($\overline{Q}_3$ = HIGH) | | | | |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

**TABLE II.**
**PARALLEL DATA ENTRY**

| $P_0 - P_3$ INPUT @ $t_n$ | Q @ $t_{n+1}$ |
|---|---|
| L | L |
| H | H |

**TABLE III.**
**SERIAL DATA ENTRY**

| D INPUT @ $t_n$ | $Q_0$ @ $t_{n+1}$ |
|---|---|
| L | L |
| H | H |

$t_n$ = Present State
$t_{n+1}$ = State after next clock
H = HIGH Voltage Level
L = LOW Voltage Level

**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| SYMBOL | PARAMETER | | 93H Min | 93H Max | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| $I_{OS}$ | Output Short Circuit Current | | -30 | -100 | mA | $V_{CC}$ = Max, $V_{OUT}$ = 0 V |
| $I_{CC}$ | Power Supply Current | XM | | 120 | mA | $V_{CC}$ = Max |
| | | XC | | 135 | | |

**AC CHARACTERISTICS:** $V_{CC}$ = +5.0 V, $T_A$ = +25° C (See Section 3 for waveforms and load configurations)

| SYMBOL | PARAMETER | 93H $C_L$ = 15 pF Min | 93H $C_L$ = 15 pF Max | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| $f_{max}$ | Maximum Shift Frequency | 45 | | MHz | Figs. 3-1, 3-8 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CP to $Q_n$ | | 16<br>21 | ns | Figs. 3-1, 3-8 |
| $t_{PHL}$ | Propagation Delay<br>$\overline{MR}$ to $Q_n$ | | 26 | ns | Figs. 3-1, 3-16 |

**AC OPERATING REQUIREMENTS:** $V_{CC}$ = +5.0 V, $T_A$ = +25° C

| SYMBOL | PARAMETER | 93H Min | 93H Max | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| $t_s$ (H)<br>$t_s$ (L) | Setup Time HIGH or LOW<br>D or $P_n$ to CP | 7.0 | | ns | Fig. 3-6 |
| $t_s$ (H)<br>$t_s$ (L) | Setup Time HIGH or LOW<br>$\overline{E}$ to CP | 17 | | | |
| $t_s$ (H)<br>$t_s$ (L) | Setup Time HIGH or LOW<br>$\overline{PE}$ to CP | 19 | | ns | Fig. 3-6 |
| $t_h$ (H)<br>$t_h$ (L) | Hold Time HIGH or LOW<br>D, $P_n$, $\overline{E}$ or $\overline{PE}$ to CP | 0 | | | |
| $t_w$ (L) | $\overline{MR}$ Pulse Width LOW | 19 | | ns | Fig. 3-16 |
| $t_{rec}$ | $\overline{MR}$ Recovery Time | 7.0 | | | |