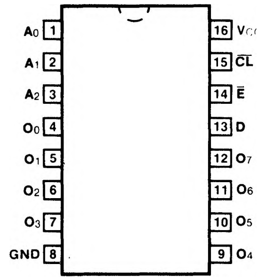
9334
93L34
8-BIT ADDRESSABLE LATCH

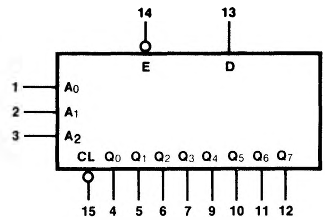
DESCRIPTION — The '34 is an 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level HIGH outputs. The device also incorporates an active LOW common clear for resetting all latches, as well as, an active LOW enable.

- **SERIAL TO PARALLEL CAPABILITY**
- **EIGHT BITS OF STORAGE WITH OUTPUT OF EACH BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY**
- **EASILY EXPANDABLE**
- **COMMON CONDITIONAL CLEAR**

CONNECTION DIAGRAMS
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	9334PC, 93L34PC		9B
Ceramic DIP (D)	A	9334DC, 93L34DC	9334DM, 93L34DM	6B
Flatpak (F)	A	9334FC, 93L34FC	9334FM, 93L34FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
A_0 — A_3	Address Inputs	1.0/1.0	0.5/0.25
D	Data Input	1.0/1.0	0.5/0.25
$\overline{E}$	Enable Input (Active LOW)	1.5/1.5	0.75/0.38
$\overline{CL}$	Clear Input (Active LOW)	1.0/1.0	0.5/0.25
Q_0 — Q_7	Parallel Latch Outputs	18/6.0	10/5.0 (3.0)

FUNCTIONAL DESCRIPTION — The '34 has four modes of operation which are shown in the Mode Select Table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the Data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the Enable should be held HIGH while the Address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the '34 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

MODE SELECT TABLE

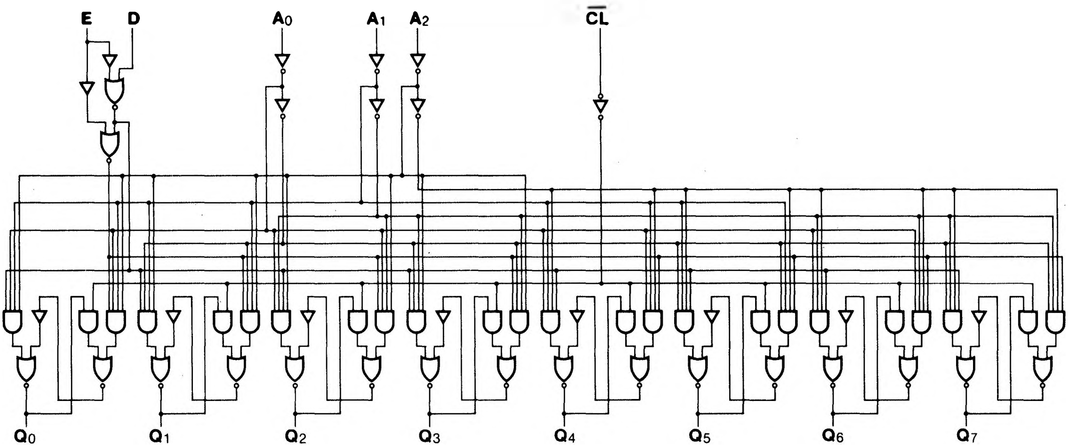
$\overline{E}$	$\overline{CL}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 8-Channel Demultiplexer
H	L	Clear

TRUTH TABLE

INPUTS					OUTPUTS								MODE
$\overline{CL}$	$\overline{E}$	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	D	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	D	L	L	L	L	L	L	
L	L	L	H	L	L	L	D	L	L	L	L	L	
•	•	•	•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	•	•	•	
L	L	H	H	H	L	L	L	L	L	L	L	D	
H	H	X	X	X	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Memory
H	L	L	L	L	D	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Addressable Latch
H	L	H	L	L	Q_{t-1}	D	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	
H	L	L	H	L	Q_{t-1}	Q_{t-1}	D	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	
•	•	•	•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	•	•	•	
H	L	H	H	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	D	

H = HIGH Voltage Level   L = LOW Voltage Level   X = Immaterial Q_{t-1} = Previous Output State

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		93XX Min	93XX Max	93L Min	93L Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		86		21	mA	V_{CC} = Max
		XC		86		26		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF Min	93XX C_L = 15 pF Max	93L C_L = 15 pF Min	93L C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n		23 24		45 42	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay D to Q_n		28 24		65 45	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n		35 35		66 66	ns	Figs. 3-1, 3-20
t_{PHL}	Propagation Delay $\overline{CL}$ to Q_n		40		55	ns	Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	93XX Min	93XX Max	93L Min	93L Max	UNITS	CONDITIONS
t_s (H)	Setup Time HIGH, D to $\overline{E}$	20		45		ns	Fig. 3-13
t_h (H)	Hold Time HIGH, D to $\overline{E}$	0		-5.0		ns	
t_s (L)	Setup Time LOW, D to $\overline{E}$	17		45		ns	
t_h (L)	Hold Time LOW, D to $\overline{E}$	0		-7.0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to $\overline{E}$	5.0 5.0		10 10		ns	Fig. 3-21
t_w (L)	$\overline{E}$ Pulse Width LOW	17		26		ns	
t_w (L)	$\overline{CL}$ Pulse Width LOW			35		ns	Fig. 3-17