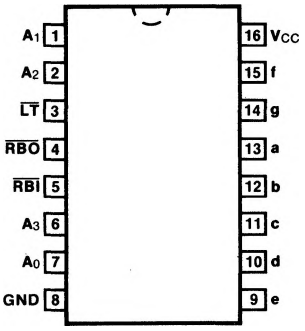
9307
7-SEGMENT DECODER

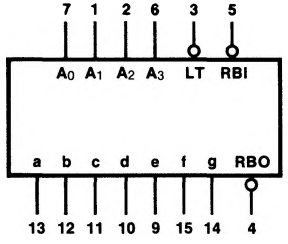
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '07 7-segment decoder is designed to accept four inputs in 8421 BCD code and provide the appropriate outputs to drive a 7-segment numerical display. The decoder can be used with 7-segment incandescent lamp, neon, electro-luminescent, or CRT numeric displays.

- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING-EDGE ZEROES**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **LAMP TEST FACILITY**
- **BLANKING INPUT**
- **ACTIVE HIGH OUTPUTS**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9307PC		9B
Ceramic DIP (D)	A	9307DC	9307DM	6B
Flatpak (F)	A	9307FC	9307FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
$A_0 - A_3$	BCD Inputs	0.25/1.0
$\overline{RBI}$	Ripple Blanking Input (Active LOW)	0.25/0.5
$\overline{LT}$	Lamp Test Input (Active LOW)	1.25/4.0
$\overline{RBO}$	Ripple Blanking Output (Active LOW)	1.75/1.5
a — g	Segment Outputs (Active HIGH)	0/6.25

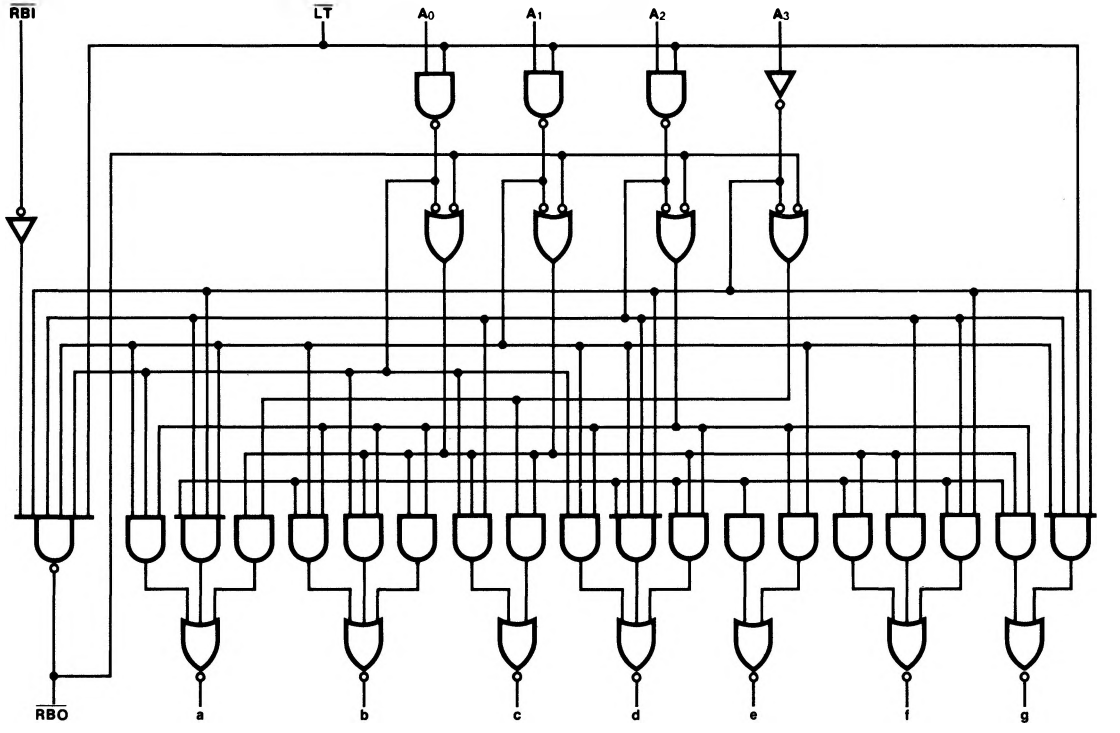
FUNCTIONAL DESCRIPTION — The '07 7-segment decoder accepts a 4-bit BCD 8421 code input and produces the appropriate outputs for selection of segments in a 7-segment matrix display used for representing the decimal numbers 0-9. The seven outputs (a, b, c, d, e, f, g) of the decoder select the corresponding segments in the matrix shown in *Figure a*. The numeric designations chosen to represent the decimal numbers are shown in *Figure b*, together with the resulting displays for input code configurations in excess of binary nine.

The decoder has active HIGH outputs so that a buffer transistor may be used directly to provide the high currents required for incandescent displays. If additional base drive current is required external resistors may be added from the supply voltage to the seven segment outputs of the decoders. If additional base drive current is required external resistors may be added from the supply voltage to the seven segment outputs of the decoders. The value of this resistor is constrained by the 10 mA current sinking capability of the output transistors of the circuit.

The device has provision for automatic blanking of the leading and/or trailing-edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading-edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and, since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing-edge zeroes.

The decoder has an active LOW input Lamp Test which overrides all other input combinations and enables a check to be made on possible display malfunctions. The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL gates.

LOGIC DIAGRAM



TRUTH TABLE

INPUTS						OUTPUTS								
$\overline{LT}$	$\overline{RBI}$	A_0	A_1	A_2	A_3	a	b	c	d	e	f	g	$\overline{RBO}$	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	
H	L	L	L	L	L	L	L	L	L	L	L	L	L	0
H	H	L	L	L	L	H	H	H	H	H	H	L	H	0
H	X	H	L	L	L	L	H	H	L	L	L	L	H	1
H	X	L	H	L	L	H	H	L	H	H	L	H	H	2
H	X	H	H	L	L	H	H	H	H	L	L	H	H	3
H	X	L	L	H	L	L	H	H	L	L	L	H	H	4
H	X	H	L	H	L	H	L	H	H	L	H	H	H	5
H	X	L	H	H	L	H	L	H	H	H	H	H	H	6
H	X	H	H	H	L	H	H	H	L	L	L	L	H	7
H	X	L	L	L	H	H	H	H	H	H	H	H	H	8
H	X	H	L	L	H	H	H	H	H	L	H	H	H	9
H	X	L	H	L	H	L	L	L	H	H	L	H	H	10
H	X	H	H	L	H	L	L	L	H	L	L	H	H	11
H	X	L	L	H	H	L	H	H	L	L	H	H	H	12
H	X	H	L	H	H	H	L	H	H	L	H	H	H	13
H	X	L	H	H	H	L	L	L	H	H	H	H	H	14
H	X	H	H	H	H	L	L	L	L	L	L	L	H	15

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

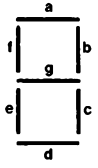


Fig. a Segment Designation

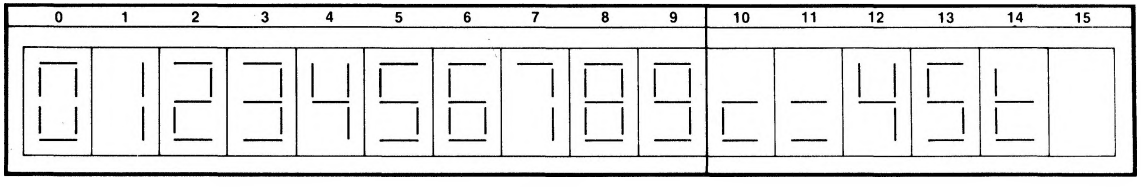


Fig. b Numerical Designations

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			93XX Min	93XX Max	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	at a—g		4.3		V	V_{CC} = Min I_{OH} = 0 mA	
		at $\overline{RBO}$	XM XC	3.0 2.7		V	V_{CC} = Min I_{OH} = -70 μA	
V_{OL}	Output LOW Voltage	at a—g	XM		0.4	V	I_{OL} = 12.5 mA	V_{CC} = Max
			XC		0.45		I_{OL} = 11.5 mA	
		at $\overline{RBO}$	XM		0.4	V	I_{OL} = 3.1 mA	
			XC		0.45		I_{OL} = 2.75 mA	
		at a—g	XM		0.4	V	I_{OL} = 10 mA	V_{CC} = Min
			XC		0.45			
		at $\overline{RBO}$	XM		0.4	V	I_{OL} = 2.4 mA	
			XC		0.45			
I_A	Available Output Current at a—g		XM	-1.0		mA	V_{OUT} = 0.85 V	V_{CC} = Min
			XC	-1.1			V_{OUT} = 0.75 V	T_A = Max
I_{OS}	Output Short Circuit Current at a—g		XM		-3.7	mA	V_{CC} = Max, T_A = +25°C V_{OUT} = 0 V	
			XC		-4.0			
I_{CC}	Power Supply Current		XM		73	mA	V_{CC} = Max	
			XC		82			

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 30 pF Min	93XX C_L = 30 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_0—A_3 or $\overline{RBI}$ to a—g or $\overline{RBO}$		750 750	ns	Fig. 3-20