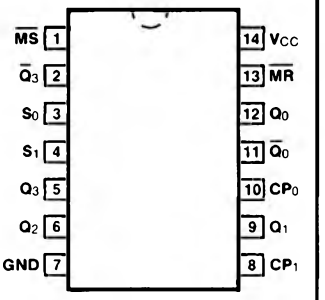
9305

VARIABLE MODULUS COUNTER

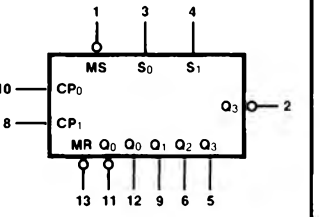
DESCRIPTION — The '05 is a monolithic, high speed, variable modulus counter circuit. It is a semisynchronous counter which can be programmed without extra logic to provide division or counting by either 2 and 4, 5, 6, 7, 8 or 10, 12, 14, 16. A binary count sequence can be obtained for all of the preceding counter modulos as well as 50% duty cycle output for dividers of 8, 10, 12, 14, 16. The device also features asynchronous overriding Master Reset and Set inputs and the negation output of the final flip-flop output which allows the cascading of stages.

- **VARIOUS BINARY COUNTING MODES**
  MODULO 2 AND MODULO 5, 6, 7, 8
  MODULO 10 (8421 BCD) 12, 14, 16
- **VARIOUS DIVISION MODES WITH 50% DUTY CYCLE OUTPUT**
  MODULO 8, 10, 12, 14, 16
- **LOGIC SELECTION OF COUNTING MODE**
- **ASYNCHRONOUS MASTER RESET ANS SET INPUTS**
- **MULTISTAGE COUNTING OPERATION**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9305PC		9A
Ceramic DIP (D)	A	9305DC	9305DM	6A
Flatpak (F)	A	9305FC	9305FM	3B

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
S_0 , S_1	Select Inputs	1.0/1.0
CP_0	First Stage Clock Pulse Input (Active Rising Edge)	1.0/1.0
CP_1	Three Stage Clock Pulse Input (Active Rising Edge)	1.0/1.0
$\overline{MS}$	Master Set Input (Active LOW)	1.0/1.0
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0
Q_0	First Stage Output	16/8.0
$\overline{Q}_0$	Complementary First Stage Output	16/8.0
$Q_1 - Q_3$	Three Stage Counter Outputs	16/8.0
$\overline{Q}_3$	Complementary Last Stage Output	20/10

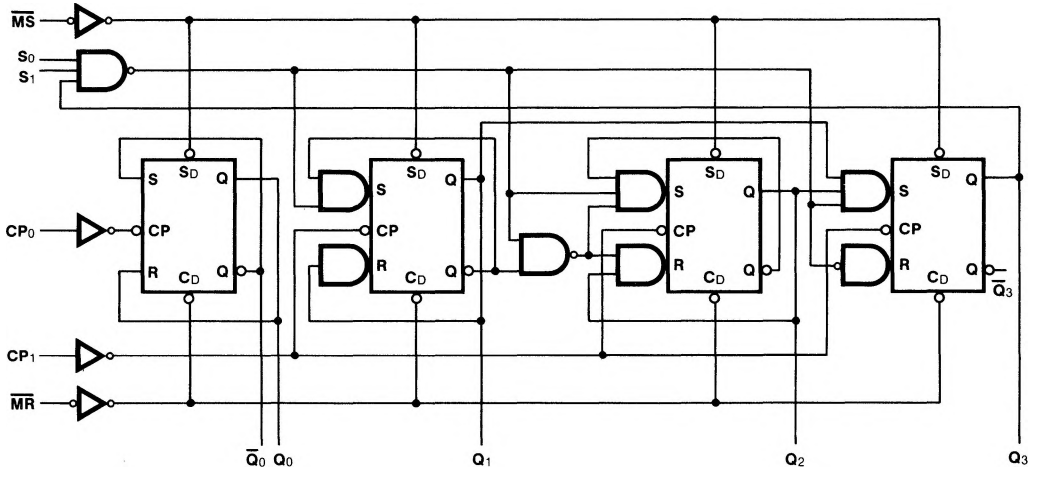
FUNCTIONAL DESCRIPTION — The '05 consists of four master/slave flip-flops which are separated into two functional units — a single toggle stage and a three stage synchronous counter. All four flip-flips change state on the LOW-to-HIGH transition of the clock. The three stage counter can be programmed with external connections to provide moduli of either 5, 6, 7 or 8. This basic configuration allows synchronous binary counting by the last three stages and independent modulo 2 operation with the first single stage.

A four stage binary counter with a modulo of 10, 12, 14 or 16 is obtained by applying the incoming clock to the single toggle stage and feeding its negation output to the clock input of the three stage counter. A 4-stage divider with 50% duty cycle output is produced by feeding the incoming clock to the three stage counter and clocking the single stage with the $\overline{Q}_3$ output. In either the binary or 50% division mode the modulo (10, 12, 14, 16) is determined by the external programming connections for the three stage counter. These 4-stage counters or dividers are not fully synchronous (semisynchronous) but have only one flip-flop ripple delay in either configuration. Counter moduli other than 10, 12, 14, 16 can be formed with a few extra gates.

Several '05 variable modulus counters programmed in any modulo can be connected together without extra logic to form asynchronous (ripple) type multistage counters. This is done by connecting the $\overline{Q}_3$ output of the less significant counter to the clock input of the following counter.

The Master Set and Reset will asynchronously set or reset all four stages when activated. The active LOW Reset input when LOW will clear the counter, overriding the clock and forcing the outputs $Q_0 - Q_3$ LOW and outputs $\overline{Q}_0$, $\overline{Q}_3$ HIGH. The active LOW Set input when LOW will preset the counter, overriding the clock and forcing the outputs $Q_0 - Q_3$ HIGH and outputs $\overline{Q}_0$, $\overline{Q}_3$ LOW. The master set provides a synchronous clear, since the first clock pulse following the asynchronous master set will reset all stages. This action is independent of the molulo programmed.

LOGIC DIAGRAM



COUNTING MODE

The following are rules specifying the external connections required for various counter and divider modulos.

ASYNCHRONOUS MODE

INPUTS		OUTPUTS					
$\overline{MS}$	$\overline{MR}$	Q_0	$\overline{Q_0}$	Q_1	$\overline{Q_2}$	Q_3	$\overline{Q_3}$
L	H	H	L	H	H	H	L
H	L	L	H	L	L	L	H
H	H	COUNT*					

*As determined by programming connections.
H = HIGH Voltage Level
L = LOW Voltage Level

PROGRAMMING CONNECTIONS FOR LAST THREE STAGES

S_0	S_1	MODULO
NC	NC	5
Q_1	NC	6
NC	Q_1	6
Q_2	NC	7
NC	Q_2	7
Q_1	Q_2	8
Q_2	Q_1	8

NC = Not Connected

CONNECTIONS FOR MODULO 10, 12, 14, 16 BINARY COUNTERS AND 50% DUTY CYCLE DIVIDERS

For Binary Counting $\overline{Q_0}$ connected to CP_1 Incoming clock to CP_0
For 50% Duty Cycle Output $\overline{Q_3}$ connected to CP_0 Incoming Clock to CP_1

ALTERNATE PROGRAMMING CONNECTIONS FOR LAST THREE STAGES**

MODULO	INPUTS		OUTPUT	AVAILABLE OUTPUT FAN-OUT
	S_0	S_1		
5	Q_3	Q_3	Q_3	14/8.0
6	Q_1	Q_1	Q_1	14/7.0
7	Q_2	Q_2	Q_2	14/7.0
8	Q_1	Q_2	Q_2	15/7.0
8	Q_2	Q_1	Q_1	15/7.0

**The alternate programming connections program the counter and conveniently terminate unused select inputs (NC). Since these inputs form the inputs to a single NAND gate (See logic diagram), their connection to the counter outputs for the various count modulos provides the indicated output drive.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		Min	Max		
I_{SC}	Output Short Circuit Current	-20	-70	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current		66	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Count Frequency	23		MHz	Modulo 16 (S_0 to Q_1, S_1 to Q_2, Q_0 to CP_1, Input to CP_0) Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP_0 to $\overline{Q}_3$ (Modulo 16 Connection)		38 48	ns	
t_{PLH} t_{PHL}	Propagation Delay CP_0 to $\overline{Q}_0$		21 30	ns	Modulo-16 Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP_1 to $\overline{Q}_3$ or $\overline{Q}_3$		23 30	ns	Modulo-8 Figs. 3-1, 3-8
t_{PLH}	Propagation Delay $\overline{MS}$ to Q_1		26	ns	Modulo-8 Figs. 3-1, 3-16
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_1		35	ns	Modulo-8 Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		Min	Max		
t_w	CP_0 Pulse Width	22		ns	Fig. 3-8
t_w	$\overline{MR}$ or $\overline{MS}$ Pulse Width	24		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MS}$ to CP_1	25		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP_1	30		ns	Fig. 3-16