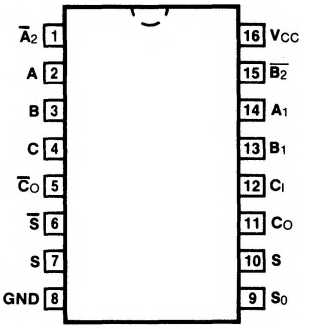
9304
DUAL FULL ADDER

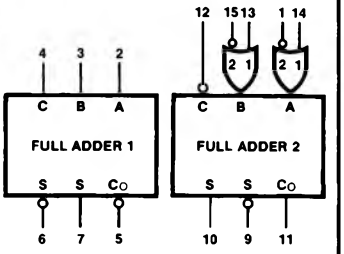
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '04 consists of two independent, binary full adders. The adders are useful in a wide variety of applications including multiple bit parallel add/serial carry addition, parity generation and checking, code conversion and majority gating.

- **MULTIFUNCTION CAPABILITY**
- **8.0 ns CARRY PROPAGATION DELAY**
- **COMPLEMENTARY INPUTS AND OUTPUTS AVAILABLE**
- **TYPICAL POWER DISSIPATION OF 150 mW**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10 %, T_A = -55°C to +125°C	
Plastic DIP (P)	A	9304PC		9B
Ceramic DIP (D)	A	9304DC	9404DM	6B
Flatpak (F)	A	9304FC	9304FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
Full Adder 1		
A, B	Operand Inputs	4.0/4.0
C_I	Carry Input	4.0/4.0
S	Sum Output	20/10
$\overline{S}$	Complementary Sum Output	20/10
$\overline{C}_O$	Carry Output (Active LOW)	14/7.0
Full Adder 2		
A_1, B_1	OR Operand Inputs (Active HIGH)	1.0/1.0
$\overline{A}_2$, $\overline{B}_2$	OR Operand Inputs (Active LOW)	4.0/4.0
$\overline{C}_I$	Carry Input (Active LOW)	4.0/4.0
S	Sum Output	20/10
$\overline{S}$	Complementary Sum Output	20/10
C_O	Carry Output (Active HIGH)	14/7.0

FUNCTIONAL DESCRIPTION — The '04 logic block consists of two separate high speed carry dependent sum full adders. This design allows a minimum carry propagation time when the adders are used in ripple carry applications. The adders are identical except that adder 2 has provision for either active HIGH or active LOW inputs at the A and B terminals. The adders produce a LOW carry and both LOW and HIGH sum with active HIGH inputs, a HIGH carry and both HIGH and LOW sum when active LOW inputs are used. This principle of duality is shown in the diagram below, where the adders are drawn as functional blocks.

TRUTH TABLES

ADDER 1

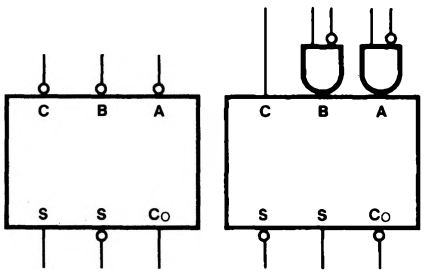
INPUTS			OUTPUTS		
$\overline{C_I}$	B	A	$\overline{C_O}$	S	$\overline{S}$
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

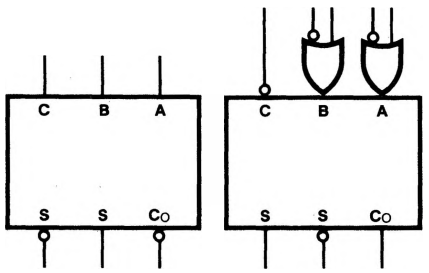
ADDER 2

INPUTS					OUTPUTS		
$\overline{C_I}$	B_1	A_1	$\overline{B_2}$	$\overline{A_2}$	C_O	S	$\overline{S}$
L	L	L	L	L	H	H	L
L	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H
L	L	L	H	H	L	H	L
L	L	H	L	L	H	H	L
L	L	H	L	H	H	H	L
L	L	H	H	L	H	L	H
L	L	H	H	H	H	L	H
L	H	L	L	L	H	H	L
L	H	L	L	H	H	L	H
L	H	L	H	L	H	H	L
L	H	L	H	H	H	L	H
L	H	H	L	L	H	H	L
L	H	H	L	H	H	H	L
L	H	H	H	L	H	H	L
L	H	H	H	H	H	H	L
H	L	L	L	L	H	L	H
H	L	L	L	H	L	H	L
H	L	L	H	L	L	H	L
H	L	L	H	H	L	L	H
H	L	H	L	L	H	L	H
H	L	H	L	H	H	L	H
H	L	H	H	L	L	H	L
H	L	H	H	H	L	H	L
H	H	L	L	L	H	L	H
H	H	L	L	H	L	H	L
H	H	L	H	L	H	L	H
H	H	L	H	H	L	H	L
H	H	H	L	L	H	L	H
H	H	H	L	H	H	L	H
H	H	H	H	L	H	L	H
H	H	H	H	H	H	L	H

ACTIVE LOW

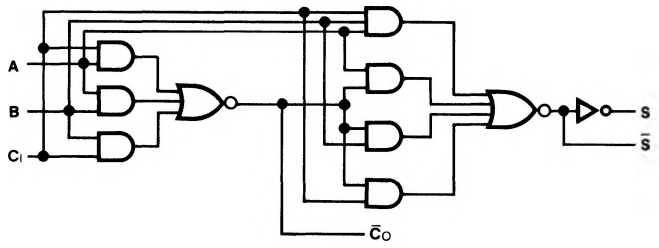


ACTIVE HIGH

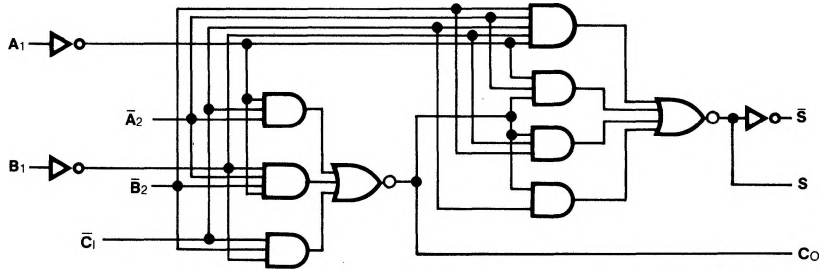


LOGIC DIAGRAM

ADDER 1



ADDER 2



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		Min	Max		
I_{SC}	Output Short Circuit Current	-20	-70	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current		55	mA	V_{CC} = Max, Pins 13 & 14 = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		C_L = 15 pF			
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to $\bar{S}$		36 35	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay C_I to C_O		13 13	ns	Figs. 3-1, 3-4