signetics

DUAL PERIPHERAL DRIVER | 75450

LINEAR INTEGRATED CIRCUITS

DESCRIPTION

The 75450 and 75450A are dual peripheral drivers designed for use in systems that employ TTL or DTL logic. These circuits feature two standard 7400 series gates and two uncommitted, high current, high voltage, npn output driver transistors.

ABSOLUTE MAXIMUM RATINGS

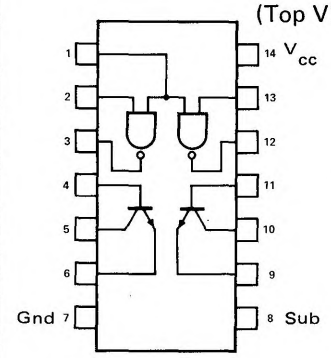
Supply Voltage	+7V
Input Voltage	+5.5V
Collector-Emitter Voltage	+30V
Continuous Collector Current	300mA
Continuous Total Power Dissipation	800mW

NOTES:

Positive Logic: $Y = \overline{AG}$ (gate only)
$C = AG$ (gate and transistor)

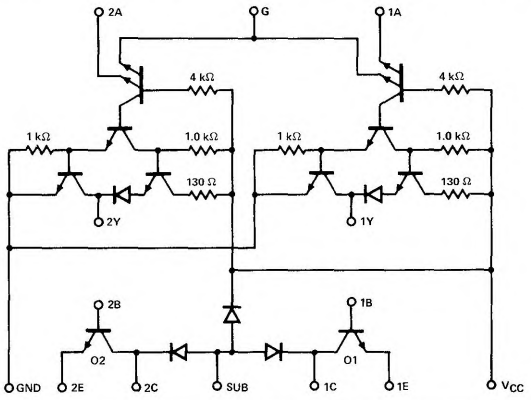
PIN CONFIGURATION

A PACKAGE
(Top View)



ORDER PART NOS.
SN75450N
SN75450AN

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS - TTL GATES (V_{CC} = 5V, T_A = 25°C)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_I	Input Clamp Voltage		V_{CC} = 4.75V, I_I = −12mA			−1.5	V
V_{OH}	High-Level Output Voltage		V_{CC} = 4.75V, V_{IL} = 0.8V, I_{OM} = −400μA	2.4	3.3		V
V_{OL}	Low-Level Output Voltage		V_{CC} = 4.75V, V_{1H} = 2V, I_{OL} = 16mA		0.22	0.4	V
I_I	Input Current at Maximum Input Voltage	Input A Input G	V_{CC} = 5.25V, V_I = 5.5V			1 2	mA
I_{IH}	High-Level Input Current	Input A Input G	V_{CC} = 5.25V, V_I = 2.4V			40 80	μA
I_{IL}	Low-Level Input Current	Input A Input G	V_{CC} = 5.25V, V_I = 0.4V			−1.6 −3.2	mA
I_{OS}	Short Circuit Output Current		V_{CC} = 5.25V	−18		−55	mA
I_{CCH}	Supply Current, High-Level Output		V_{CC} = 5.25V, V_I = 0		2	4	mA
I_{CCL}	Supply Current, Low-Level Output		V_{CC} = 5.25V, V_I = 5V		6	11	mA

ELECTRICAL CHARACTERISTICS - OUTPUT TRANSISTORS (Cont'd)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)\ CBO}$ Collector-Base Breakdown Voltage	$I_C = 100\mu A$, $I_E = 0$	35			V
$V_{(BR)\ CER}$ Collector-Emitter Breakdown Voltage	$I_C = 100\mu A$, $R_{BE} = 500\Omega$	30			V
$V_{(BR)\ EBO}$ Emitter-Base Breakdown Voltage	$I_E = 100\mu A$, $I_C = 0$	5			V
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 3V$, $I_C = 100mA$, $T_A = 25°C$	25			
	$V_{CE} = 3V$, $I_C = 300mA$, $T_A = 25°C$	30			
	$V_{CE} = 3V$, $I_C = 100mA$ $T_A = 0°C$	20			
	$V_{CE} = 3V$, $I_C = 300mA$, $T_A = 0°C$	25			
V_{BE} Base-Emitter Voltage	$I_B = 10mA$, $I_C = 100mA$		0.85	1	V
	$I_B = 30mA$, $I_C = 300mA$		1.05	1.2	V
$V_{CE\ (sat)}$ Collector-Emitter Saturation Voltage	$I_B = 10mA$, $I_C = 100mA$		0.25	0.4	V
	$I_B = 30mA$, $I_C = 300mA$		0.5	0.7	V

SWITCHING CHARACTERISTICS - TTL GATES ($V_{CC} = 5V$, $T_A = 25°C$)

PARAMETER	TEST CONDITIONS	75450			75450A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
TTL GATES								
t_{PLH} Propagation Delay Time Low-to-High-Level Output	$C_L = 15pF$, $R_L = 400\Omega$		12	22		20		ns
t_{PHL} Propagation Delay Time, High-to-High-Level Output			8	15		8		ns
OUTPUT TRANSISTORS								
t_D Delay Time	$I_C = 200mA$, $I_{B(1)} = 20mA$		8	15		8		ns
t_r Rise Time	$I_{B(2)} = -40mA$,		12	20		12		ns
t_s Storage Time	$V_{BE(off)} = -1V$		7	15		7		ns
t_f Fall Time	$C_L = 15pF$, $R_L = 50$		6	15		6		ns
GATES AND TRANSISTORS COMBINED								
t_{PLH} Propagation Delay Time, Low-to-High-Level Output	$I_C = 200mA$, $C_L = 15pF$, $R_L = 50$		17			40		ns
t_{PHL} Propagation Delay Time, High-to-Low-Level Output			16			25		ns
t_{TLH} Transition Time, Low-to-High-Level Output			7			10		ns
t_{THL} Transition Time, High-to-Low-Level Output			9			12		ns