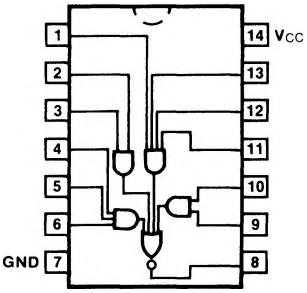
54S/74S65

4-2-3-2-INPUT AND-OR-INVERT GATE

(With Open-Collector Output)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	74S65PC		9A
Ceramic DIP (D)	A	74S65DC	54S65DM	6A
Flatpak (F)	A	74S65FC	54S65FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74S (U.L.) HIGH/LOW
Inputs	1.25/1.25
Outputs	OC[1]/12.5

DC AND AC CHARACTERISTICS: See Section 3[2]

SYMBOL	PARAMETER	54/74S Min	54/74S Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply Current		11	mA	V_{IN} = 0 V	V_{CC} = Max
I_{CCL}			16		Note 3	
t_{PLH}	Propagation Delay	2.0	7.5	ns	Figs. 3-2, 3-4	
t_{PHL}		2.0	8.5			

[1]OC — Open Collector
[2]DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
[3]I_{CCL} is measured with all inputs of one gate open and remaining inputs grounded.