

DESCRIPTION

The 54/74S200/201 and 54/74S301 are read/write memory arrays which feature either open collector or tri-state output options for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and pnp input transistors, which reduces input loading to 25 μ A for a high level and -250 μ A (S54S200/201/301) or -100 μ A (N74S200/201/301) for a low level.

The additional feature of output blanking during Write (\bar{D}_O terminal "H" or "Hi-Z" state) permits \bar{D}_O and D_{IN} terminals to share a common I/O line to reduce system interconnections. These devices have fast read access and write cycle times, and thus are ideally suited in high speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

They are available in both the commercial and military temperature ranges. The commercial temperature range (0°C to +75°C) is specified as N74S200/201/301, F or N, and the military temperature range (-55°C to +125°C) is specified as S54S200/201/301, F only.

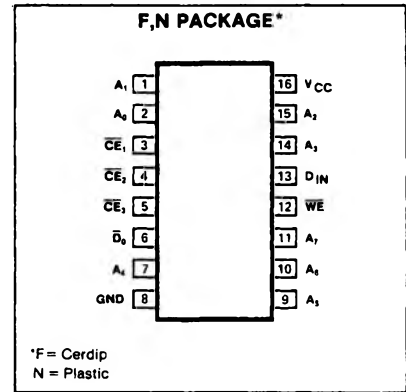
FEATURES

- Address access time:
N74S200/201/301: 50ns max
S54S200/201/301: 70ns max
- Write cycle time:
N74S200/201/301: 50ns max
S54S200/201/301: 60ns max
- Power dissipation : 1.5mW/bit typ
- Input loading:
N74S200/201/301: -100 μ A max
S54S200/201/301: -250 μ A max
- Output blanking during Write
- On-chip address decoding
- Output option:
54/74S200/201: Tri-state
54/74S301: Open collector
- Schottky clamped
- TTL compatible

APPLICATIONS

- Buffer memory
- Writable control store
- Memory mapping
- Push down stack
- Scratch pad

PIN CONFIGURATION

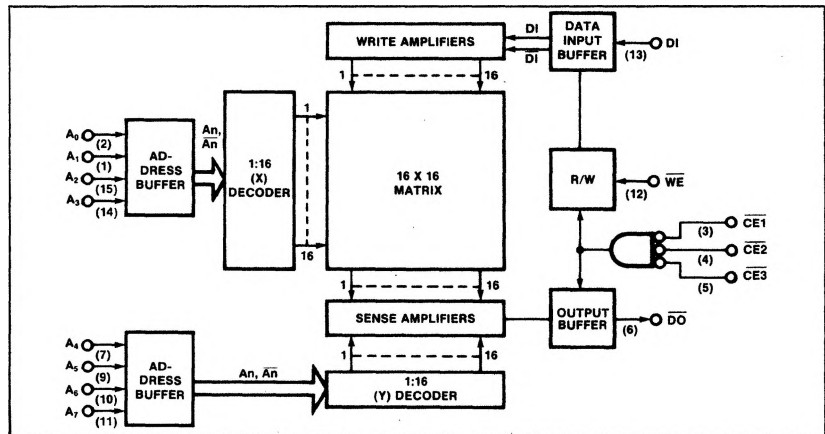


TRUTH TABLE

MODE	\overline{CE}^*	\overline{WE}	D _{IN}	D _{OUT}	
				54/74S301	54/74S200/201
Read	0	1	X	Stored Data	Stored Data
Write "0"	0	0	0	1	High-Z
Write "1"	0	0	1	1	High-Z
Disabled	1	X	X	1	High-Z

*"0" = All \overline{CE} inputs low; "1" = One or more \overline{CE} inputs high.
X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
V _{OUT} Output voltage		Vdc
V _O High (54/74S301)	+5.5	
V _O Off-state (54/74S200/201)	+5.5	
T _A Temperature range		°C
T _A Operating		
N74S200/201/301	0 to +70	
S54S200/201/301	-55 to +125	
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS N74S200/201/301: 0°C ≤ T_A ≤ +70°C, 4.75V ≤ V_{CC} ≤ 5.25V
S54S200/201/301: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS	N74S200/201/301			S54S200/201/301			UNIT
		Min	Typ ¹	Max	Min	Typ ¹	Max	
V _{IL} Input voltage Low ²	V _{CC} = Min			0.85			0.8	V
V _{IH} Input voltage High ²	V _{CC} = Max	2.0			2.0			
V _{IC} Clamp ^{2,3}	V _{CC} = Min, I _{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
V _{OL} Output voltage Low ^{2,4}	V _{CC} = Min I _{OL} = 16mA		0.35	0.45		0.30	0.50	V
V _{OH} Output voltage High (N74S200/201) ^{2,5}	I _{OH} = 10.3mA	2.4			2.4			
V _{OH} Output voltage High (S54S200/201) ^{2,5}	I _{OH} = -5.2mA							
I _I Input current ³ At V _{IN} Max	V _{CC} = Max V _{IN} = 5.5V			1			1	mA
I _{IL} Input current Low	V _{IL} = 0.45V		-10	-100		-10	-250	μA
I _{IH} Input current High	V _{IH} = 2.7V		1	25		1	25	μA
I _{OLK} Output current Leakage (54/74S301) ⁶	V _{IH} = 2V, V _O = 5.5V		1	40		1	50	μA
I _{O(OFF)} Output current Hi-Z state (54/74S200/201) ⁶	V _{CC} = Max, V _O = 5.5V		1	40		1	100	μA
I _{OS} Output current Short circuit (54/74S200/201) ⁷	V _{IH} = 2V, V _O = 0.4V V _{CC} = Max, V _O = 0V	-30		-40	-30		-100	mA
I _{CC} V _{CC} supply current ⁸	V _{CC} = Max V _{CC} = Max, T _A = +125°C		80	130		80	130	mA
C _{IN} Capacitance Input	V _{CC} = 5.0V V _{IN} = 2.0V		5			5		pF
C _{OUT} Capacitance Output	V _{OUT} = 2.0V		8			8		pF

AC ELECTRICAL CHARACTERISTICS $R_L = 270\Omega$, $C_L = 15pF$, See ac test load
 N74S200/201/301: $0^\circ C \leq T_A \leq +70^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$
 S54S200/201/301: $-55^\circ C \leq T_A \leq +125^\circ C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER ⁹	TO	FROM	TEST CONDITIONS	N74S200/201			S54S200/201			UNIT
				Min	Typ ¹	Max	Min	Typ ¹	Max	
t _{PLH} Access time B,D,E Low to high		Address			40	50		40	70	ns
t _{PHL} High to low										
t _{PLH} Low to high		Address	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$							ns
t _{ZL} Enable time Low C,D,F,G	Output	Chip enable				35			45	
t _{ZH} High C,D,F,G										
t _{PHL} High to low C,D,E	Output	Chip enable	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$							ns
t _{LZ} Disable time Low C,D,F,G	Output	Chip enable	$C_L=5pF$			20			30	
t _{HZ} High C,D,F,G										
t _{PLH} Low to high C,D,E	Output	Chip enable	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$							
t _{PHL} High to low C,D,E	Output	Write enable								
t _{LZ} Low D,G	Output	Write enable	$C_L=5pF$			30			40	
t _{HZ} High D,G										
t _{ZL} Sense recovery time Low D,F						40			50	ns
t _{ZH} High D,F										
t _{SR} Sense D										
t _w Pulse width H Write enable			$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$	40			50			ns
t _s Setup and hold time D	Write enable	Address		0			0			ns
t _H Setup time Hold time	Address	Write enable		10			10			
t _s Setup time Hold time	Write enable	Address	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$							
t _s Setup time Hold time	Write enable	Data		40			50			
t _H Setup time Hold time	Data	Write enable		10			10			
t _s Setup time Hold time	Write enable	Data	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$							
t _s Setup time Hold time	Write enable	Chip enable		0			0			
t _H Setup time Hold time	Chip enable	Write enable		0			0			
t _s Setup time Hold time	Write enable	Chip enable	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$							
t _H Setup time Hold time	Chip enable	Write enable								

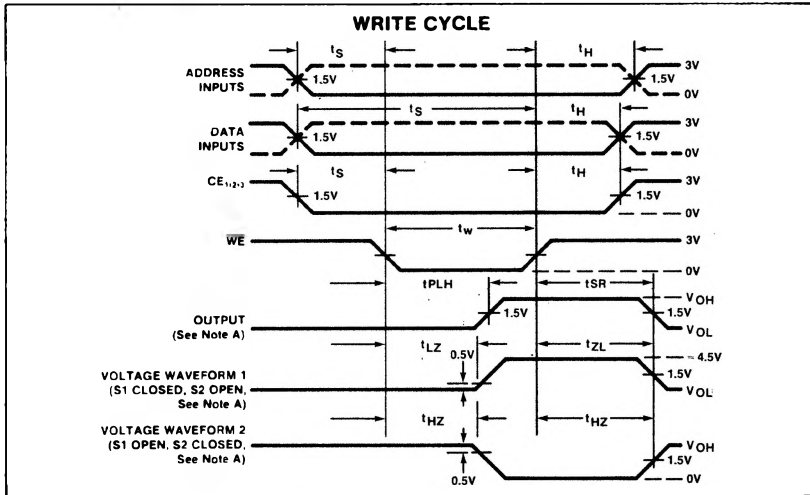
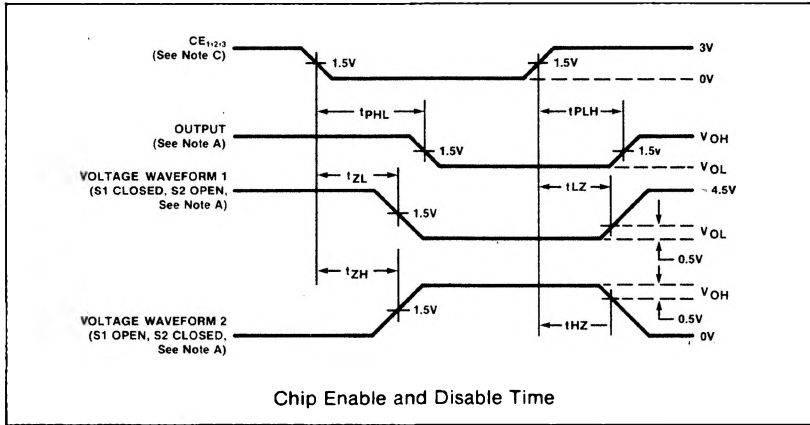
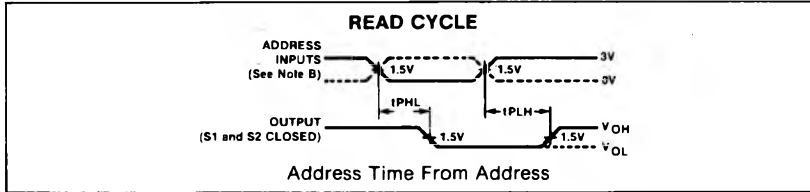
AC ELECTRICAL CHARACTERISTICS(Cont'd) $R_L = 270\Omega$, $C_L = 15\text{pF}$, See ac test loadN74S200/201/301: $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$ S54S200/201/301: $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER ⁹	TO	FROM	TEST CONDITIONS	N74S301			S54S301			UNIT
				Min	Typ ¹	Max	Min	Typ	Max	
t _{PLH} Access time ^{B,D,E} Low to high t _{PHL} High to low		Address							ns	
	t _{PLH} Low to high	Address	$R_{L1}=270\Omega$, $R_{L2}=1\text{k}\Omega$		40	50		40		70
t _{ZL} Enable time Low ^{C,D,F,G} t _{ZH} High ^{C,D,F,G}	Output	Chip enable							ns	
	t _{PHL} High to low ^{C,D,E}	Output	Chip enable	$R_{L1}=270\Omega$, $R_{L2}=1\text{k}\Omega$		35				45
t _{LZ} Disable time Low ^{C,D,F,G} t _{HZ} High ^{C,D,F,G}	Output	Chip enable	$C_L=5\text{pF}$						ns	
	t _{PLH} Low to high ^{C,D,E} t _{PHL} High to low ^{C,D,E}	Output	Chip enable Write enable	$R_{L1}=270\Omega$, $R_{L2}=1\text{k}\Omega$		20 30				30 40
t _{LZ} Low ^{D,G} t _{HZ} High ^{D,G}	Output	Write enable	$C_L=5\text{pF}$						ns	
	t _{ZL} Sense recovery time Low ^{D,F} t _{ZH} High ^{D,F}									ns
t _{SR} Sense ^D						40			50	
t _w Pulse width ^H Write enable			$R_{L1}=270\Omega$, $R_{L2}=1\text{k}\Omega$	40			50		ns	
t _s Setup and hold time ^D t _h Setup time Hold time	Write enable	Address							ns	
	t _s Setup time t _h Hold time	Write enable Address	Address Write enable	$R_{L1}=270\Omega$, $R_{L2}=1\text{k}\Omega$	0 10		0 10			
t _s Setup time t _h Hold time	Write enable	Data							ns	
	t _s Setup time t _h Hold time	Write enable Data	Data Write enable	$R_{L1}=270\Omega$, $R_{L2}=1\text{k}\Omega$	40 10		50 10			
t _s Setup time t _h Hold time	Write enable	Chip enable							ns	
	t _s Setup time t _h Hold time	Write enable Chip enable	Chip enable Write enable	$R_{L1}=270\Omega$, $R_{L2}=1\text{k}\Omega$	0 0		0 0			

NOTES

- All typical values are at $V_{CC} = 5\text{V}$, $T_A = +25^\circ\text{C}$.
- All voltage values are with respect to network ground terminal.
- Test each input one at a time.
- Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC} .
- Measured with logic stored, and V_{IL} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
- Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
- Duration of the short circuit should not exceed 1 second.
- I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
- See timing diagram notes.

TIMING DIAGRAMS



NOTES

- A. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
- B. When measuring delay times from address inputs, the chip enable inputs are low and the write enable input is high.
- C. When measuring delay times from chip enable inputs, the address inputs are steady-state and the write enable input is high.
- D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5\text{ns}$, $t_f \leq 2.5\text{ns}$, $\text{PRR} \leq 1\text{MHz}$, and $Z_{\text{OUT}} = 50\Omega$.
- E. t_{PLH} propagation delay time, low-to-high level output, t_{PHL} propagation delay time, high-to-low level output.
- F. t_{ZH} propagation delay time, Hi-Z to high level output, t_{ZL} propagation delay time, Hi-Z to low level output.
- G. t_{HZ} propagation delay time, high level to Hi-Z output, t_{LZ} propagation delay time, low level to Hi-Z output.
- H. Minimum required to guarantee a Write into the slowest bit.

TEST LOAD CIRCUITS

