

DESCRIPTION

This family of Read/Write Random Access Memories is ideal for use in scratch pad and high-speed buffer memory applications.

These products are fully decoded memory arrays with separate input and output lines. They feature pnp inputs and 1 chip enable line for ease of memory expansion.

During Write, the outputs of each product assume a logic state by the output access time and the truth table.

The family is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify the N prefix, and for the military temperature range (-55°C to +125°C) specify the S prefix. The 54/74S89/189 military temperature range product is ordered as S54S89/189. The S grade product is supplied in the F package only.

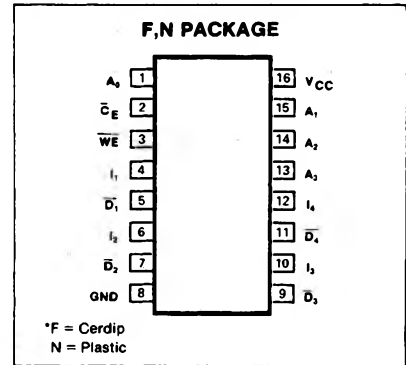
FEATURES

- **Output access time:**
 N82S25: 50ns
 N3101A: 35ns
 N54/74S89: 50ns
 N54/74S189: 35ns
- **Power dissipation:** 6.25mW/bit, typ
- **Input loading:**
 N grade: -100µA max
 S grade: -150µA max
- **On-chip address decoding**
- **Output options:**
 82S25: Open collector
 3101A: Open collector
 54/74S89: Open collector
 54/74S189: Tri-state
- **Schottky processed**
- **TTL compatible**

APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

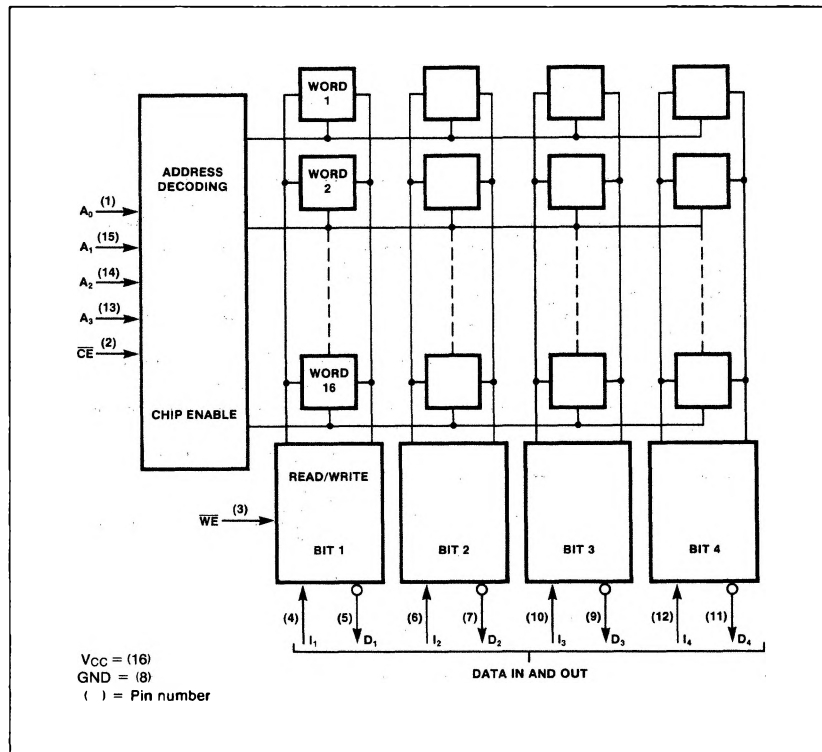
PIN CONFIGURATION



TRUTH TABLE

	\overline{CE}	\overline{WE}	D _{IN}	82S25	3101A	54/74S89	54/74S189
				DATA OUT			
Read	0	1	X	Stored data	Stored data	Stored data	Stored data
Write "0"	0	0	0	1	1	1	Hi-Z
Write "1"	0	0	1	1	1	0	Hi-Z
Disable	1	X	X	1	1	1	Hi-Z

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER ¹		RATING	UNIT
V _{CC}	Supply voltage	+7	Vdc
V _{IN}	Input voltage	+5.5	Vdc
V _{OH}	Output voltage High	+5.5	Vdc
T _A	Temperature range Operating		°C
	N grade	0 to +75	
	S grade	-55 to +125	
T _{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS N grade: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S grade: 55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS	N GRADE			S GRADE			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp V _{CC} = Min V _{CC} = Max I _{IN} = -12mA, V _{CC} = Min	2.0	-1.0	.85 -1.5	2.0	-1.0	.80 -1.5	V
V _{OL} V _{OH}	Output voltage Low ^{3,4} High (54/74S189) I _{OUT} = 16mA, V _{CC} = Min I _{OUT} = 2mA	2.4	0.35	0.45	2.4	0.35	0.5	V
I _{IL} I _{IH}	Input current Low High V _{IN} = 0.45V V _{IN} = 5.5V		-10	-100 10		-10	-150 25	μA
I _{OLK} I _{OS} I _{O(OFF)}	Output current Leakage Short circuit (54/74S189) Hi-Z (54/74S189) CE = high, V _{OUT} = 5.5V, V _{CC} = Min V _{OUT} = 0V 2.4 ≥ V _{OUT} ≥ 0.4V		<1 -30	100 -100 ±50		<1 -30	100 -100 ±50	μA mA μA
I _{CC}	Supply current ⁴ 82S25, 54/74S89 3101A 54/74S189		80 80 80	105 105 110		80 80 80	120 120 110	mA
C _{IN} C _{OUT}	Capacitance Input Output V _{CC} = 5.0V V _{IH} = 2.0V V _{OUT} = 2.0V, CE = high		5 8			5 8		pF

AC ELECTRICAL CHARACTERISTICS

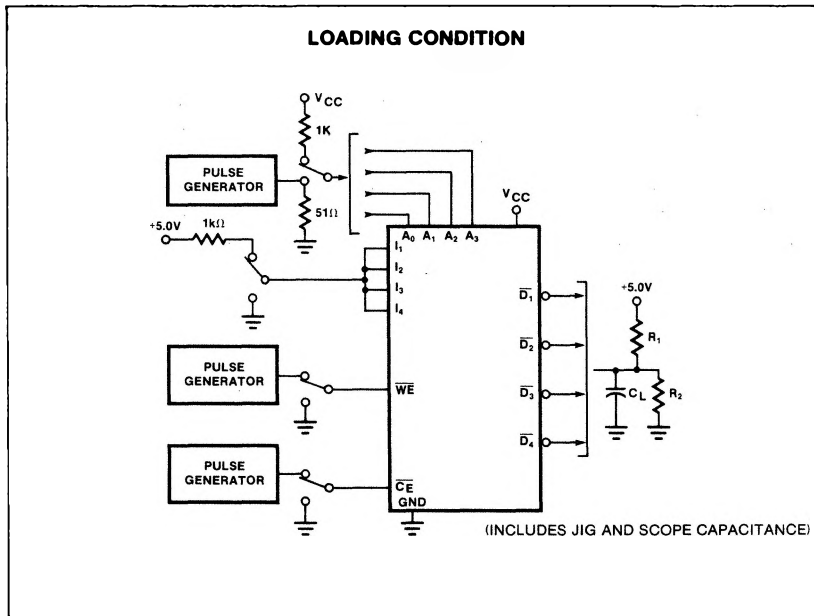
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, See ac test load
N grade: $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$
S grade: $-55^\circ C \leq T_A \leq +125^\circ C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER	TO	FROM	N82S25, N74S89			S82S25, S54S89			N3101A, N74S189			S3101A, S54S189			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
T_{AA} Access time				35	50		35	60		25	35		25	50	ns
T_{CE} Address Chip enable				20	35		20	35		12	17		12	25	ns
T_{CD} Disable time	Output	Chip enable		20	35		20	35		12	17		12	25	ns
T_{WD} Response time	Output	Write enable		20	25		20	30		15	25		15	30	ns
T_{WR} Write recovery time				35	50		35	60		22	35		22	40	ns
Setup and hold time															ns
T_{WSA} Setup time	Write enable	Address	5	-8		10	-8		0			0			
T_{WHA} Hold time			5	0		10	0		0		10				
T_{WSD} Setup time	Write enable	Data in	30	15		30	15		25			30			
T_{WHD} Hold time			5	-3		10	-3		0		10				
T_{WSC} Setup time	Write enable	\overline{CE}	0	-5		0	-5		0			0			
T_{WHC} Hold time			5	0		5	0		0		0		0		
Pulse width															ns
T_{WP} Write enable ⁵			30	18		30	18		25			30	1		

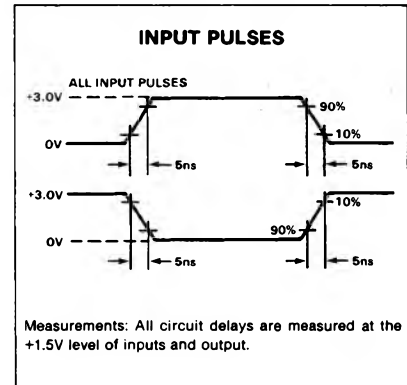
NOTES

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Typical values are at $V_{CC} = +5.0V$ and $T_A = +25^\circ C$.
3. Output sink current is supplied through a resistor to V_{CC} .
4. All sense outputs in low state.
5. To guarantee a Write into the slowest bit.
6. Positive current is defined as into the terminal referenced.
7. Positive logic definition: high = +5.0V, low = GND.
8. Test each input one at a time.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



TIMING DIAGRAMS

