

# 54S/74S109 54LS/74LS109

## DUAL JK̄ POSITIVE EDGE-TRIGGERED FLIP-FLOP

**DESCRIPTION** — The '109 consists of two high speed, completely independent transition clocked JK̄ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK̄ design allows operation as a D flip-flop (refer to '74 data sheet) by connecting the J and K inputs together. The '109 is functionally equivalent to the 9024.

**TRUTH TABLE**

INPUTS		OUTPUTS	
@ t <sub>n</sub>		@ t <sub>n</sub> + 1	
J	K	Q	Q̄
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

**Asynchronous Inputs:**

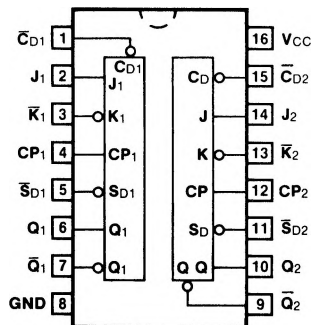
- LOW input to  $\bar{S}_D$  sets Q to HIGH level
- LOW input to  $\bar{C}_D$  sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both Q and  $\bar{Q}$  HIGH

t<sub>n</sub> = Bit time before clock pulse.  
t<sub>n</sub> + 1 = Bit time after clock pulse.  
H = HIGH Voltage Level  
L = LOW Voltage Level

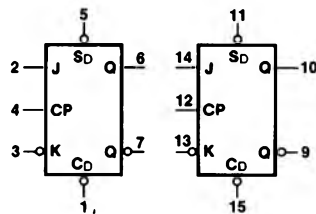
**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	74S109PC, 74LS109PC		9A
Ceramic DIP (D)	A	74S109DC, 74LS109DC	54S109DM, 54LS109DM	6A
Flatpak (F)	A	74S109FC, 74LS109FC	54S109FM, 54LS109FM	3I

**CONNECTION DIAGRAM  
PINOUT A**



**LOGIC SYMBOL**

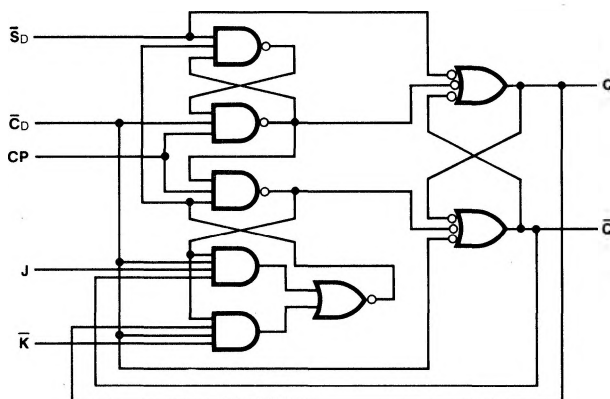


V<sub>CC</sub> = Pin 16  
GND = Pin 8

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J <sub>1</sub> , J <sub>2</sub> , $\bar{K}_1$ , $\bar{K}_2$	Data Inputs	1.25/1.25	0.5/0.25
CP <sub>1</sub> , CP <sub>2</sub>	Clock Pulse Inputs (Active Rising Edge)	2.5/2.5	1.0/0.5
$\bar{C}_D1$ , $\bar{C}_D2$	Direct Clear Inputs (Active LOW)	5.0/5.0	1.0/1.0
$\bar{S}_D1$ , $\bar{S}_D2$	Direct Set Inputs (Active LOW)	2.5/2.5	1.0/0.5
Q <sub>1</sub> , Q <sub>2</sub> , $\bar{Q}_1$ , $\bar{Q}_2$	Outputs	25/12.5	10/5.0 (2.5)

LOGIC DIAGRAM (one half shown)



## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I <sub>CC</sub>	Power Supply Current	52		8.0		mA	V <sub>CC</sub> = Max, V <sub>CP</sub> = 0 V

AC CHARACTERISTICS: V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		C <sub>L</sub> = 15 pF R <sub>L</sub> = 280 Ω		C <sub>L</sub> = 15 pF			
		Min	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	75		30		MHz	Figs. 3-1, 3-8
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay C <sub>Pn</sub> to Q <sub>n</sub> or Q̄ <sub>n</sub>	9.0 11		25 35		ns	Figs. 3-1, 3-8
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay C̄ <sub>Dn</sub> or S̄ <sub>Dn</sub> to Q <sub>n</sub> or Q̄ <sub>n</sub>	6.0 12		15 35		ns	V <sub>CP</sub> ≥ 2.0 V Figs. 3-1, 3-10
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay C̄ <sub>Dn</sub> or S̄ <sub>Dn</sub> to Q <sub>n</sub> or Q̄ <sub>n</sub>	6.0 12		15 24		ns	V <sub>CP</sub> ≤ 0.8 V Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time J <sub>n</sub> or K̄ <sub>n</sub> to C <sub>Pn</sub>	6.0		18		ns	Fig. 3-6
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time J <sub>n</sub> or K̄ <sub>n</sub> to C <sub>Pn</sub>	0		0		ns	
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP <sub>n</sub> Pulse Width	7.0 6.5		20 13.5		ns	
t <sub>w</sub> (L)	C̄ <sub>Dn</sub> or S̄ <sub>Dn</sub> Pulse Width LOW	6.0		15		ns	Fig. 3-10