National Semiconductor

74LVQ151
Low Voltage 8-Input Multiplexer
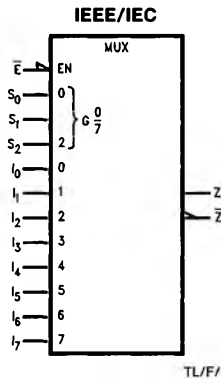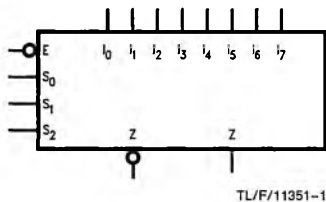
General Description

The LVQ151 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one line of data from up to eight sources. The LVQ151 can be used as a universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.
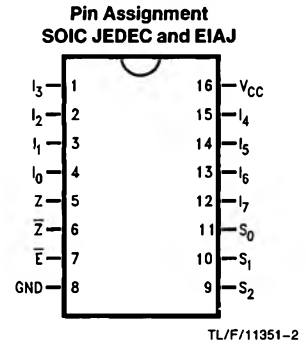
Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/Aerospace applications

Ordering Code: See Section 11

Logic Symbols

TL/F/11351–1

IEEE/IEC

TL/F/11351–4

Connection Diagram

Pin Assignment
SOIC JEDEC and EIAJ

	Pin		Pin	
I_3	1	16	V_{CC}	
I_2	2	15	I_4	
I_1	3	14	I_5	
I_0	4	13	I_6	
Z	5	12	I_7	
$\bar{Z}$	6	11	S_0	
$\bar{E}$	7	10	S_1	
GND	8	9	S_2	

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Pin Names	Description
I_0–I_7	Data Inputs
S_0–S_2	Select Inputs
$\bar{E}$	Enable Input
Z	Data Output
$\bar{Z}$	Inverted Data Output

Truth Table

Inputs				Outputs	
$\bar{E}$	S_2	S_1	S_0	$\bar{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\bar{I}_0$	I_0
L	L	L	H	$\bar{I}_1$	I_1
L	L	H	L	$\bar{I}_2$	I_2
L	L	H	H	$\bar{I}_3$	I_3
L	H	L	L	$\bar{I}_4$	I_4
L	H	L	H	$\bar{I}_5$	I_5
L	H	H	L	$\bar{I}_6$	I_6
L	H	H	H	$\bar{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

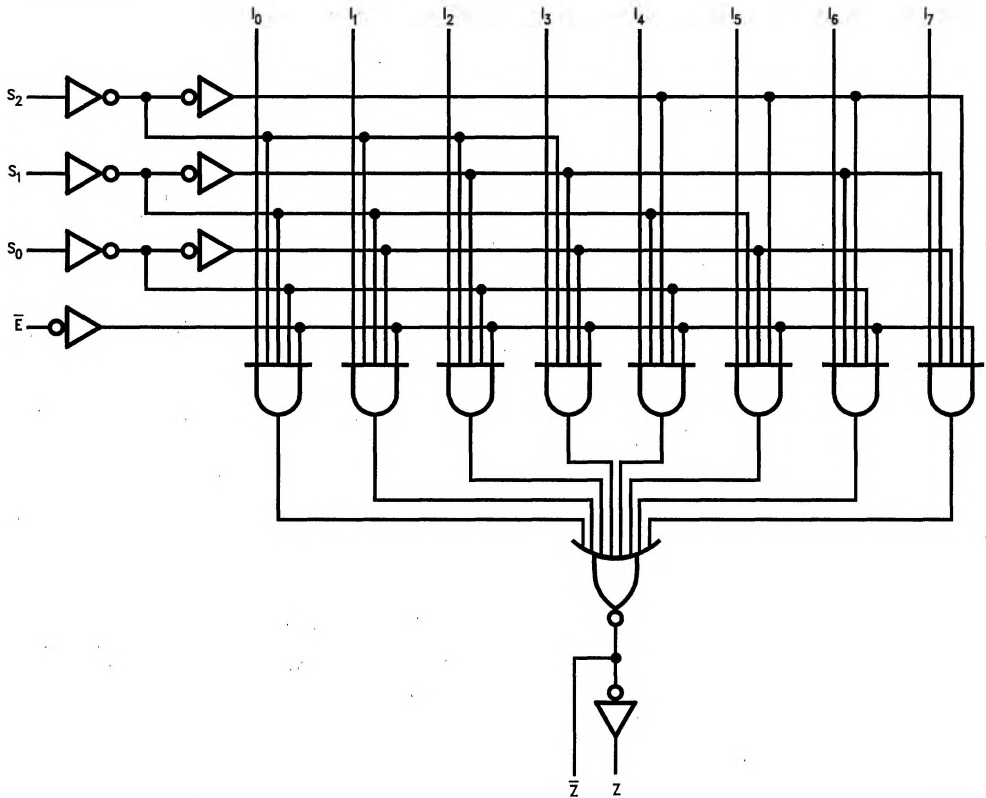|	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ151SC 74LVQ151SCX	74LVQ151SJ 74LVQ151SJX
See NS Package Number	M16A	M16D

Functional Description

The LVQ151 is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both true and complementary outputs are provided. The Enable input ($\overline{E}$) is active LOW. When it is not activated, the complementary output is HIGH and the true output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 +$$
$$I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 +$$
$$I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 +$$
$$I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet \overline{S}_2)$$

The LVQ151 provides the ability, in one package to select from eight sources of data or control information. By proper manipulation of the inputs, the LVQ151 can provide any logic function of four variables and its complement.

Logic Diagram

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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	$-0.5V$ to $+7.0V$
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	$+20$ mA
DC Input Voltage (V_I)	$-0.5V$ to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	$+20$ mA
DC Output Voltage (V_O)	$-0.5V$ to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	± 200 mA
Storage Temperature (T_{STG})	$-65°C$ to $+150°C$
DC Latch-Up Source or Sink Current	± 100 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	$-40°C$ to $+85°C$
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ151 $T_A = +25°C$	74LVQ151 $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$
		3.0		2.58	2.48	V	*$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12$ mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$
		3.0		0.36	0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12$ mA
I_{IN}	Maximum Input Leakage Current	3.6		± 0.1	± 1.0	μA	$V_I = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

LVQ151

DC Characteristics (Continued)

Symbol	Parameter	V_CC (V)	74LVQ151 T_A = +25°C	74LVQ151 T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits		
I_OLD	†Minimum Dynamic Output Current	3.6		36	mA	V_OLD = 0.8V Max (Note 1)
I_OHD		3.6		−25	mA	V_OHD = 2.0V (Note 1)
I_CC	Maximum Quiescent Supply Current	3.6	4.0	40.0	μA	V_IN = V_CC or GND
V_OLP	Quiet Output Maximum Dynamic V_OL	3.3	0.8		V	(Notes 2 & 3)
V_OLV	Quiet Output Minimum Dynamic V_OL	3.3	−0.8		V	(Notes 2 & 3)
V_IHD	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0	V	(Notes 2 & 4)
V_ILD	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8	V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_ILD), 0V to threshold (V_IHD), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_CC (V)	74LVQ151 T_A = +25°C C_L = 50 pF			74LVQ151 T_A = −40°C to +85°C C_L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t_PLH	Propagation Delay S_n to Z or Z̄	2.7	3.0	13.8	25.3	3.0	28.0	ns
		3.3 ±0.3	3.0	11.5	18.0	3.0	20.0	
t_PHL	Propagation Delay S_n to Z or Z̄	2.7	2.5	14.4	25.3	2.5	28.0	ns
		3.3 ±0.3	2.5	12.0	18.0	2.5	20.0	
t_PLH	Propagation Delay Ē to Z or Z̄	2.7	2.5	9.6	18.3	2.0	20.0	ns
		3.3 ±0.3	2.5	8.0	13.0	2.0	14.0	
t_PHL	Propagation Delay Ē to Z or Z̄	2.7	1.5	10.2	18.3	1.5	20.0	ns
		3.3 ±0.3	1.5	8.5	13.0	1.5	14.0	
t_PLH	Propagation Delay I_n to Z or Z̄	2.7	2.5	11.4	19.7	2.0	22.0	ns
		3.3 ±0.3	2.5	9.5	14.0	2.0	15.5	
t_PHL	Propagation Delay I_n to Z or Z̄	2.7	2.5	11.4	21.1	2.0	23.0	ns
		3.3 ±0.3	2.5	9.5	15.0	2.0	16.0	
t_OSHL, t_OSLH	Output to Output Skew* Data to Output	2.7		1.0	1.5		1.5	ns
		3.3 ±0.3		1.0	1.5		1.5	

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_OSHL) or LOW to HIGH (t_OSLH). Parameter guaranteed by design.

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Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	45	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.