

DATA SHEET

74LV245

Octal bus transceiver (3-State)

Product specification
Supersedes data of 1997 Feb 19
IC24 Data Handbook

1998 Apr 20

Octal bus transceiver (3-State)

74LV245

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Typical V_{OLP} (output ground bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_{amb} = 25^{\circ}\text{C}$
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_{amb} = 25^{\circ}\text{C}$
- Output capability: bus driver
- I_{CC} category: MSI

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^{\circ}\text{C}$; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay A_n to B_n ; B_n to A_n	$C_L = 15$ pF; $V_{CC} = 3.3$ V	7.0	ns
C_I	Input capacitance		3.5	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per buffer	$V_{CC} = 3.3$ V $V_I = \text{GND to } V_{CC}$, note 1	40	pF

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; C_L = output load capacitance in pF;

f_o = output frequency in MHz; V_{CC} = supply voltage in V;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic DIL	-40°C to $+125^{\circ}\text{C}$	74LV245 N	74LV245 N	SOT146-1
20-Pin Plastic SO	-40°C to $+125^{\circ}\text{C}$	74LV245 D	74LV245 D	SOT163-1
20-Pin Plastic SSOP Type II	-40°C to $+125^{\circ}\text{C}$	74LV245 DB	74LV245 DB	SOT339-1
20-Pin Plastic TSSOP Type I	-40°C to $+125^{\circ}\text{C}$	74LV245 PW	74LV245PW DH	SOT360-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	DIR	Direction
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	Data inputs/outputs
10	GND	Ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B_0 to B_7	Data inputs/outputs
19	\overline{OE}	Output enable input (active LOW)
20	V_{CC}	Positive supply voltage

DESCRIPTION

The 74LV245 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT245.

The 74LV245 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The 74LV245 features an output enable (\overline{OE}) input for easy cascading and a send/receive (DIR) input for direction control. \overline{OE} controls the outputs so that the buses are effectively isolated.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
\overline{OE}	DIR	A_n	B_n
L	L	$A = B$	Inputs
L	H	Inputs	$B = A$
H	X	Z	Z

NOTES:

H = HIGH voltage level

L = LOW voltage level

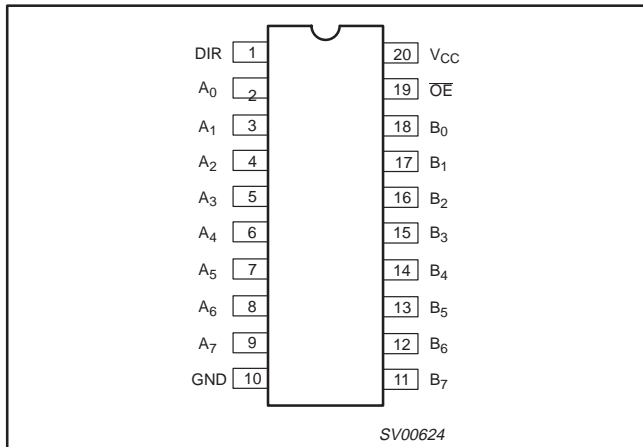
X = don't care

Z = high impedance OFF-state

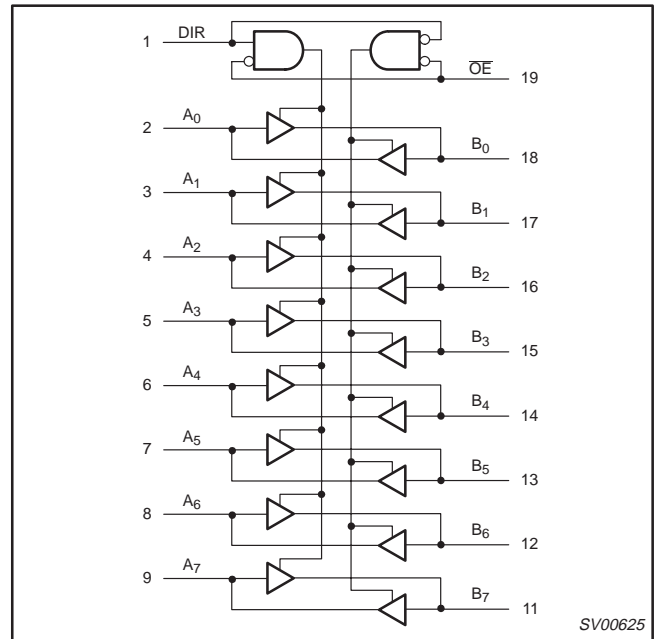
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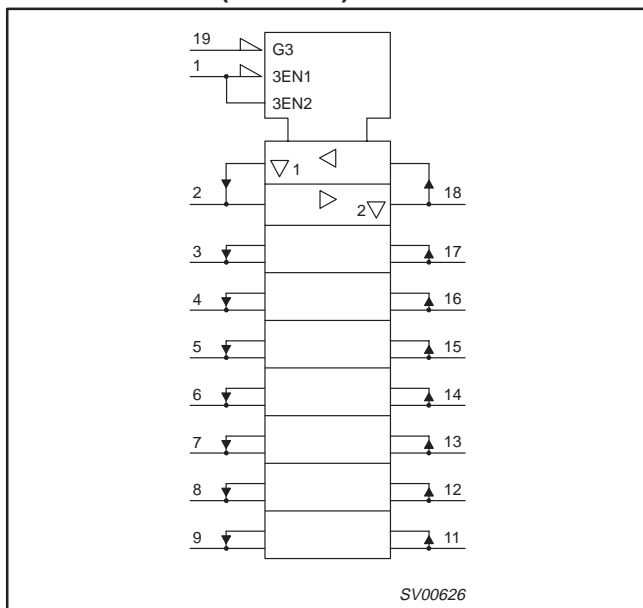
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 1.0V$ to $2.0V$ $V_{CC} = 2.0V$ to $2.7V$ $V_{CC} = 2.7V$ to $3.6V$ $V_{CC} = 3.6V$ to $5.5V$	– – – –	– – – –	500 200 100 50	ns/V

NOTE:

- The LV is guaranteed to function down to $V_{CC} = 1.0V$ (input levels GND or V_{CC}); DC characteristics are guaranteed from $V_{CC} = 1.2V$ to $V_{CC} = 5.5V$.

ABSOLUTE MAXIMUM RATINGS^{1, 2}

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND},$ $\pm I_{CC}$	DC V_{CC} or GND current for types with – bus driver outputs		70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP ¹	MAX	MIN	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	0.9			0.9		V
		V _{CC} = 2.0V	1.4			1.4		
		V _{CC} = 2.7 to 3.6V	2.0			2.0		
		V _{CC} = 4.5 to 5.5V	0.7 * V _{CC}			0.7 * V _{CC}		
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			0.3		0.3	V
		V _{CC} = 2.0V			0.6		0.6	
		V _{CC} = 2.7 to 3.6V			0.8		0.8	
		V _{CC} = 4.5 to 5.5			0.3 * V _{CC}		0.3 * V _{CC}	
V _{OH}	HIGH level output voltage; all outputs	V _{CC} = 1.2V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA		1.2				V
		V _{CC} = 2.0V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	1.8	2.0		1.8		
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	2.5	2.7		2.5		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	2.8	3.0		2.8		
		V _{CC} = 4.5V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	4.3	4.5		4.3		
V _{OH}	HIGH level output voltage; BUS driver outputs	V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; -I _O = 8mA	2.40	2.82		2.20		V
		V _{CC} = 4.5V; V _I = V _{IH} or V _{IL} ; -I _O = 16mA	3.60	4.20		3.50		
V _{OL}	LOW level output voltage; all outputs	V _{CC} = 1.2V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0				V
		V _{CC} = 2.0V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
		V _{CC} = 4.5V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
V _{OL}	LOW level output voltage; BUS driver outputs	V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 8mA		0.20	0.40		0.50	V
		V _{CC} = 4.5V; V _I = V _{IH} or V _{IL} ; I _O = 16mA		0.35	0.55		0.65	
I _I	Input leakage current	V _{CC} = 5.5V; V _I = V _{CC} or GND			1.0		1.0	µA
I _{OZ}	3-State output OFF-state current	V _{CC} = 5.5V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND			5		10	µA
I _{CC}	Quiescent supply current; MSI	V _{CC} = 5.5V; V _I = V _{CC} or GND; I _O = 0			20.0		160	µA
ΔI _{CC}	Additional quiescent supply current	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V			500		850	µA

NOTE:1. All typical values are measured at T_{amb} = 25°C.

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AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 1\text{K}\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				-40 to +85 °C			-40 to +125 °C		
				$V_{CC}(\text{V})$	MIN	TYP ¹	MAX	MIN	
t_{PHL}/t_{PLH}	Propagation delay A_n to B_n ; B_n to A_n	Figures 1	1.2		45	28			ns
			2.0		15	28		34	
			2.7		11	19		24	
			3.0 to 3.6		9 ²	16		20	
			4.5 to 5.5		8 ³	11		14	
t_{PZH}/t_{PZL}	3-State output enable time OE to A_n ; OE to B_n	Figures 2	1.2		55				ns
			2.0		19	31		39	
			2.7		14	23		29	
			3.0 to 3.6		10 ²	18		23	
			4.5 to 5.5		8.5 ³	14		18	
t_{PHZ}/t_{PLZ}	3-State output disable time OE to A_n ; OE to B_n	Figures 2	1.2		65				ns
			2.0		24	32		39	
			2.7		18	24		29	
			3.0 to 3.6		14 ²	20		24	
			4.5 to 5.5		11.5 ³	16		19	

NOTES:

1. Unless otherwise stated, all typical values are measured at $T_{\text{amb}} = 25^\circ\text{C}$
2. Typical values are measured at $V_{CC} = 3.3\text{V}$.
3. Typical values are measured at $V_{CC} = 5.0\text{V}$.

AC WAVEFORMS

$V_M = 1.5\text{V}$ at $V_{CC} \geq 2.7\text{V}$ and $\leq 3.6\text{V}$
 $V_M = 0.5\text{V} \times V_{CC}$ at $V_{CC} < 2.7\text{V}$ and $\geq 4.5\text{V}$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_X = V_{OL} + 0.3\text{V}$ at $V_{CC} \geq 2.7\text{V}$ and $\leq 3.6\text{V}$
 $V_X = V_{OL} + 0.1 \times V_{CC}$ at $V_{CC} < 2.7\text{V}$ and $\geq 4.5\text{V}$
 $V_Y = V_{OH} - 0.3\text{V}$ at $V_{CC} \geq 2.7\text{V}$ and $\leq 3.6\text{V}$
 $V_Y = V_{OH} - 0.1 \times V_{CC}$ at $V_{CC} < 2.7\text{V}$ and $\geq 4.5\text{V}$

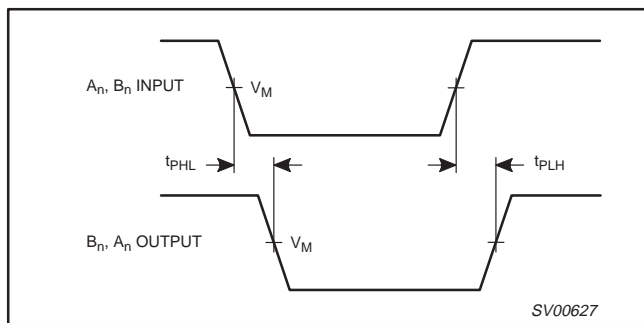


Figure 1. Input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

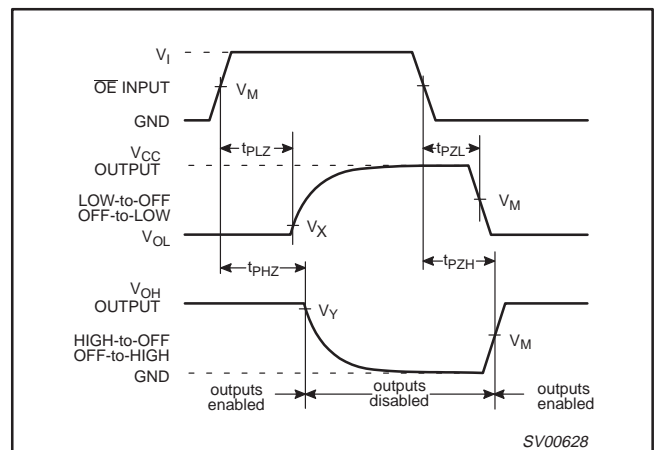


Figure 2. 3-State enable and disable times.

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TEST CIRCUIT

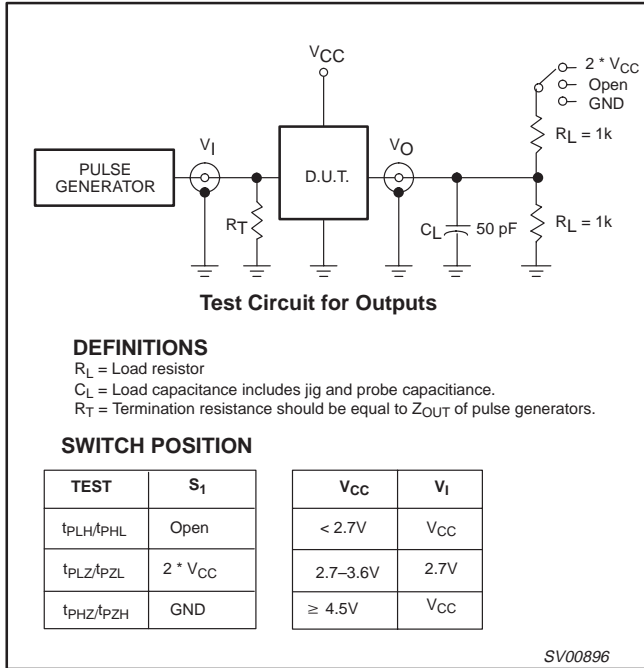


Figure 3. Load circuitry for switching times.

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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1




DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

Octal bus transceiver (3-State)

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

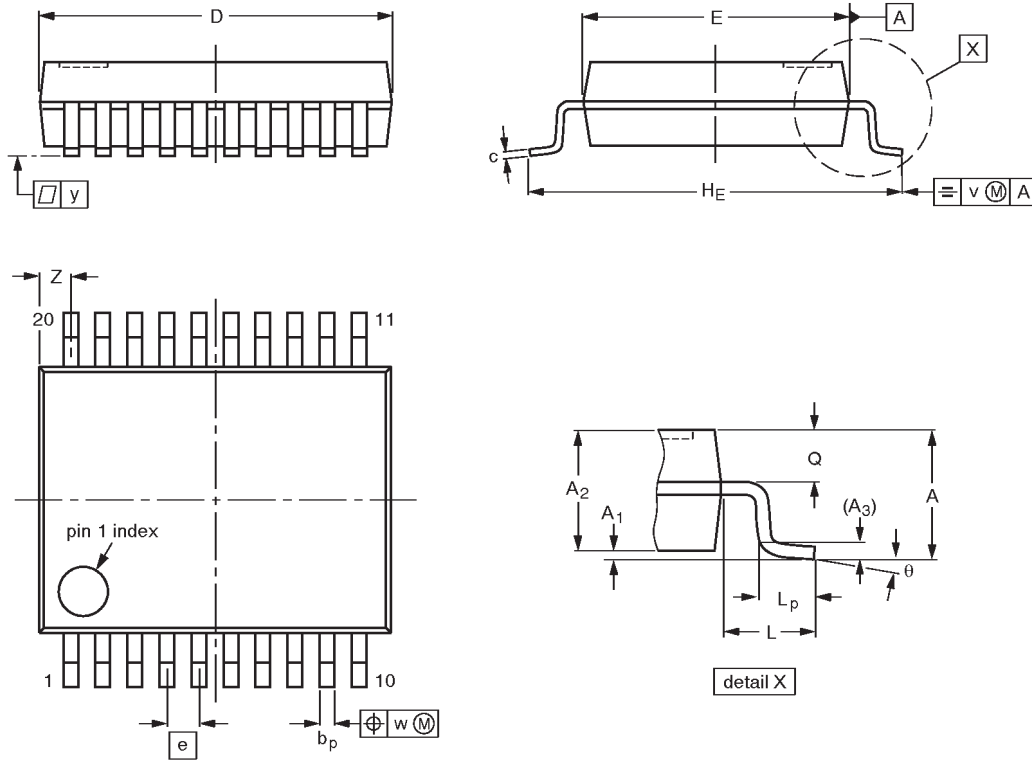
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

Octal bus transceiver (3-State)

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04

Octal bus transceiver (3-State)

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				-93-06-16- 95-02-04

Octal bus transceiver (3-State)

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DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
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<i>Product Specification</i>	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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