

# 54/7489 54LS/74LS89

## 64-BIT RANDOM ACCESS MEMORY (With Open-Collector Outputs)

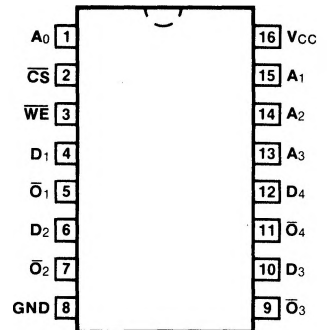
**DESCRIPTION** — The '89 a high speed, low power 64-bit Random Access Memory organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading, and addresses are fully decoded on-chip. Outputs are open-collector type and are in the off (HIGH) state when both the Chip Select (CS) and Write Enable (WE) are HIGH. For all other combinations of CS and WE the outputs are active, presenting the complement of either the stored data (READ mode) or the information present on the D inputs.

- OPEN-COLLECTOR OUTPUTS FOR WIRED-AND APPLICATIONS
- BUFFERED INPUTS MINIMIZE LOADING
- ADDRESS DECODING ON-CHIP
- DIODE CLAMPED INPUTS MINIMIZE RINGING

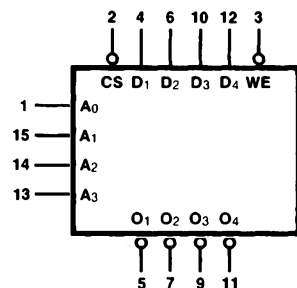
**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	7489PC, 74LS89PC		9B
Ceramic DIP (D)	A	7489DC, 74LS89DC	5489DM, 54LS89DM	7B
Flatpak (F)	A	7489FC, 74LS89FC	5489FM, 54LS89FM	4L

### CONNECTION DIAGRAM PINOUT A



### LOGIC SYMBOL



V<sub>CC</sub> = Pin 16  
GND = Pin 8

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
A <sub>0</sub> — A <sub>3</sub>	Address Inputs	1.0/1.0	0.5/0.013
CS	Chip Select Input (Active LOW)	1.0/1.0	0.5/0.013
WE	Write Enable Input (Active LOW)	1.0/1.0	0.5/0.013
D <sub>1</sub> — D <sub>4</sub>	Data Inputs	1.0/1.0	0.5/0.013
O <sub>1</sub> — O <sub>4</sub>	Inverted Data Outputs	OC*/7.5	OC*/10 (5.0)

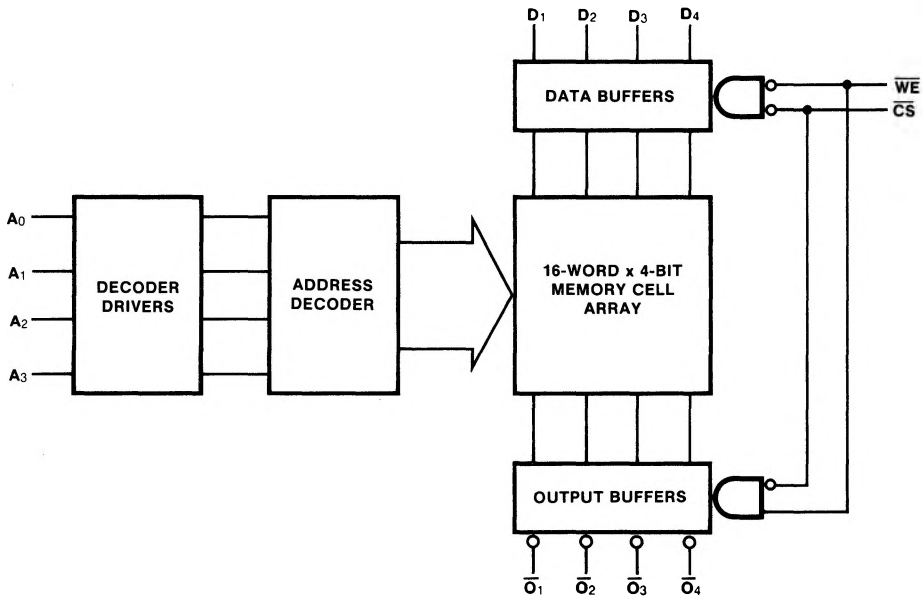
\*OC — Open Collector

**FUNCTION TABLE**

INPUTS		OPERATION	CONDITION OF OUTPUTS
CS	WE		
L	L	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Entry	Undetermined
H	H	Hold	(Off) HIGH

H = HIGH Voltage Level  
L = LOW Voltage Level

**LOGIC DIAGRAM**



**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS	
		Min	Max	Min	Max			
I <sub>OH</sub>	Output HIGH Current	20		20		μA	V <sub>CC</sub> = Min, V <sub>OH</sub> = 5.5 V	
V <sub>OL</sub>	Output LOW Voltage	0.4				V	I <sub>OL</sub> = 12 mA	V <sub>CC</sub> = Min
		0.45				V	I <sub>OL</sub> = 16 mA	
		XM, XC		0.4		V	I <sub>OL</sub> = 8.0 mA	V <sub>CC</sub> = Min
XC		0.5		V	I <sub>OL</sub> = 16 mA			
I <sub>CC</sub>	Power Supply Current	105		40		mA	V <sub>CC</sub> = Min, $\overline{CS}$ = Gnd	
C <sub>o</sub>	Off-State Output Capacitance	4.0*		4.0*		pF	V <sub>O</sub> = 2.4 V, f = 1 MHz	

**AC CHARACTERISTICS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS	
		C <sub>L</sub> = 30 pF		C <sub>L</sub> = 15 pF				
		R <sub>L</sub> = 300 Ω		R <sub>L</sub> = 2 kΩ				
		Min	Max	Min	Max			
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CS to $\overline{O}_n$	50		10*		ns	Figs. 3-2, 3-5 '89 has 600 Ω to Gnd	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> to $\overline{O}_n$	60		37*		ns	Figs. 3-2, 3-20 '89 has 600 Ω to Gnd	
t <sub>rec</sub>	Recovery Time $\overline{WE}$ to $\overline{O}_n$	70		30*		ns	Figs. 3-2, 3-4, 3-5 '89 has 600 Ω to Gnd	

**AC OPERATING REQUIREMENTS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS	
		Min	Max	Min	Max			
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time HIGH or LOW D <sub>n</sub> to $\overline{WE}$	40	40	25*	25*	ns	Fig. 3-13	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time HIGH or LOW A <sub>n</sub> to $\overline{WE}$	0	0	10*	10*	ns	Fig. 3-21	
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time HIGH or LOW D <sub>n</sub> or A <sub>n</sub> to $\overline{WE}$	5.0	5.0	0*	0*	ns	Figs. 3-13, 3-21	
t <sub>w</sub> (L)	$\overline{WE}$ Pulse Width LOW	40		25*		ns	Fig. 3-21	

\*Typical Value