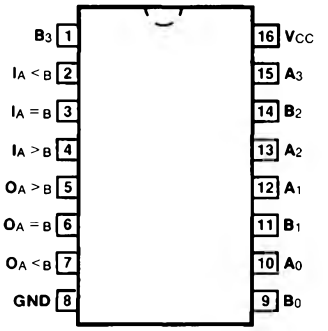
54/7485
54LS/74LS85
4-BIT MAGNITUDE COMPARATOR

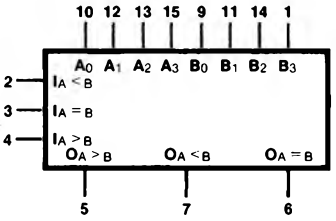
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '85 is a high speed, expandable 4-bit magnitude comparator which compares two 4-bit words in any monotonic code (binary, BCD or other) and generates three outputs: A less than B, A greater than B, and A equal to B. Three expansion inputs allow serial (ripple) expansion over any word length without external gates.

- **EASILY EXPANDABLE**
- **BINARY OR BCD COMPARISON**
- **A > B, A < B, A = B OUTPUTS AVAILABLE**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

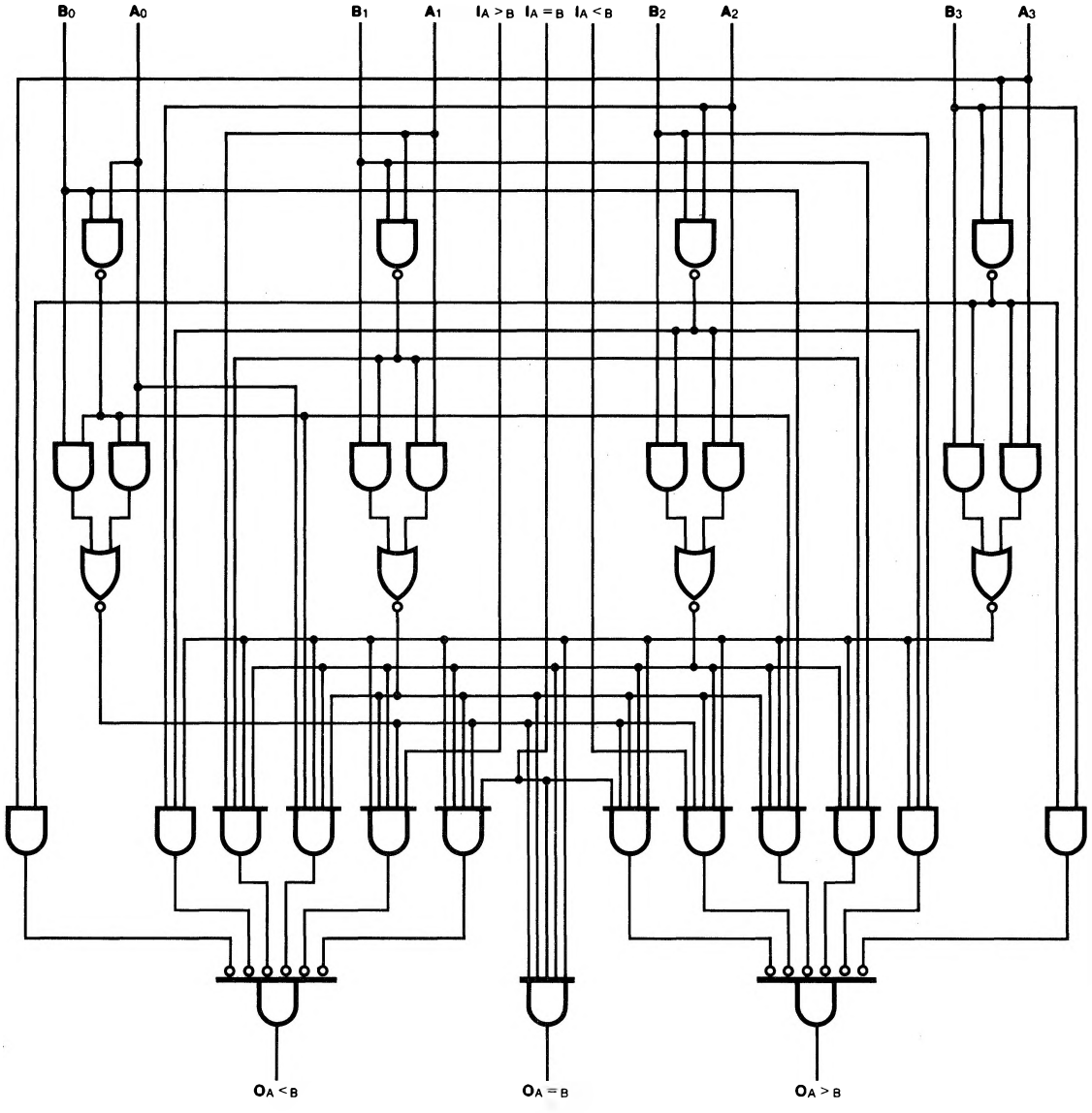
PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7485PC, 74LS85PC		9B
Ceramic DIP (D)	A	7485DC, 74LS85DC	5485DM, 54LS85DM	6B
Flatpak (F)	A	7485FC, 74LS85FC	5485FM, 54LS85FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	Word A Inputs	3.0/3.0	1.5/0.75
$B_0 - B_3$	Word B Inputs	3.0/3.0	1.5/0.75
$I_{A=B}$	A = B Expansion Input	3.0/3.0	1.5/0.75
$I_{A<B}$, $I_{A>B}$	A < B, A > B Expansion Inputs	1.0/1.0	0.5/0.25
$O_{A>B}$	A Greater Than B Output	10/10	10/5.0 (2.5)
$O_{A<B}$	A Less Than B Output	10/10	10/5.0 (2.5)
$O_{A=B}$	A Equal B Output	10/10	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION—The '85 compares two 4-bit words (A, B). Each word has four parallel inputs (A_0—A_3, B_0—B_3) of which A_3 and B_3 are the most significant. Three expander inputs ($I_{A>B}$, $I_{A<B}$, $I_{A=B}$) allow cascading without external gates. The three outputs ($O_{A>B}$, $O_{A<B}$, $O_{A=B}$) have only two gate delays from the expander inputs, thus reducing the delay time when units are cascaded for long words. The $I_{A=B}$ input to the least significant position must be held HIGH for proper compare operation. For serial (ripple) expansion, the A > B, A < B and A = B outputs are connected respectively to the $I_{A>B}$, $I_{A<B}$, and $I_{A=B}$ inputs of the next most significant comparator.

LOGIC DIAGRAM



TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3 > B_3$	X	X	X	X	X	X	H	L	L
$A_3 < B_3$	X	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	X	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	H	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	H	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

APPLICATIONS — *Figure a* shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in *Figure b* six levels of device delay result when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table I.

TABLE I

WORD LENGTH	NUMBER OF PKGS.
1-4 Bits	1
5-24 Bits	2-6
25-120 Bits	8-31

NOTE:
The 54LS/74LS85 can be used as a 5-bit comparator only when the outputs are used to drive the A_0 — A_3 and B_0 — B_3 inputs of another 54LS/74LS85 as shown in Figure 2 in positions #1, 2, 3, and 4.

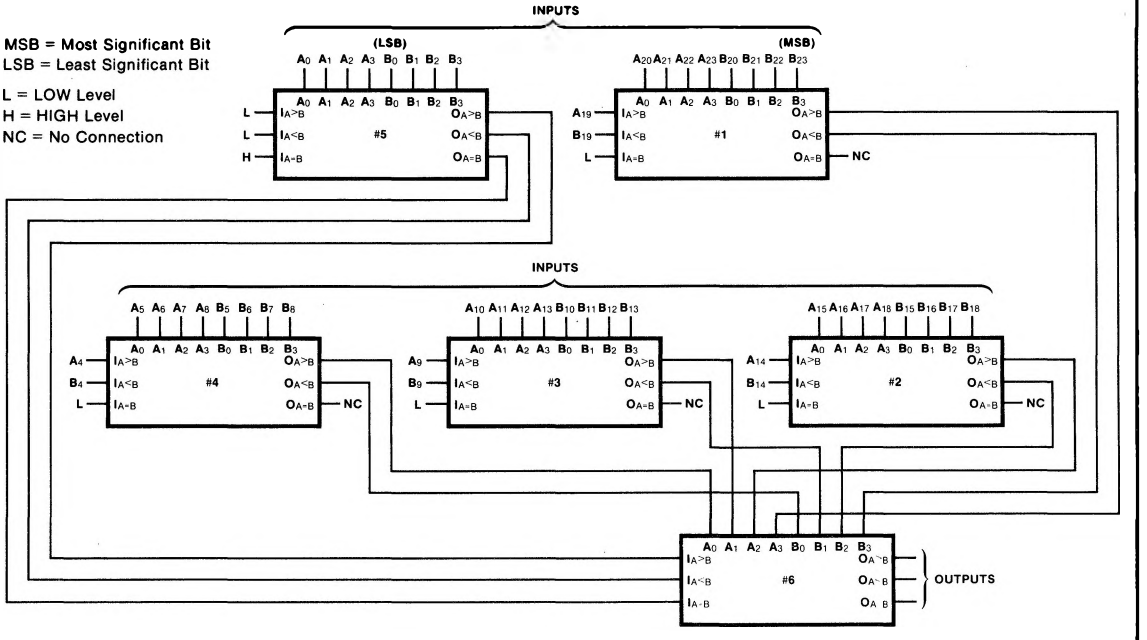
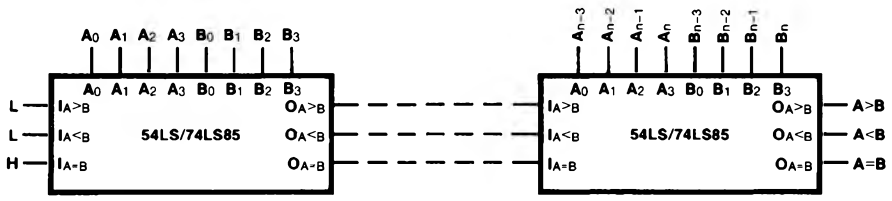


Fig. a Comparison of Two 24-Bit Words



L = LOW Level
H = HIGH Level

Fig. b Comparison of Two n-Bit Words

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	XM	-20	-55	-20	-100	mA	V_{CC} = Max
		XC	-18	-55				
I_{CC}	Power Supply Current			88		20	mA	V_{CC} = Max $I_{A=B}$ = Gnd Other Inputs Open

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to $O_{A>B}$ or $O_{A<B}$		26 30		36 30	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to $O_{A=B}$		35 30		45 45	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay A_n I_{xx} to $O_{A>B}$ or $O_{A<B}$		11 17		22 17	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay $I_{A=B}$ to $O_{A=B}$		20 17		22 17	ns	Figs. 3-1, 3-5