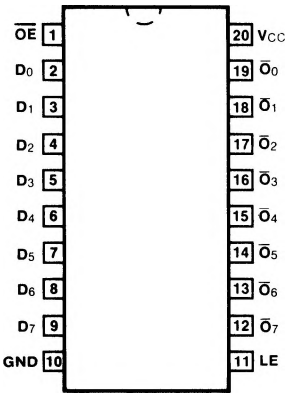
563

# 54LS/74LS563

## OCTAL D-TYPE LATCH

(With 3-State Outputs)

**CONNECTION DIAGRAM**
PINOUT A

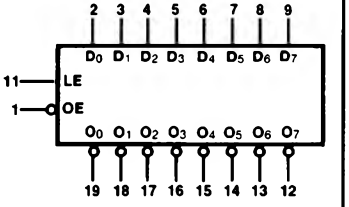



**DESCRIPTION** — The '563 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

This device is functionally indentical to the 'LS573, but has inverted outputs. For truth tables, discussion of operations and ac and dc specifications, please refer to the 'LS373 data sheet, but note that the data to output delays are 5.0 ns longer for the 'LS563 than for the 'LS373.

- **INPUTS AND OUTPUTS ON OPPOSITE SIDES OF PACKAGE ALLOWING EASY INTERFACE WITH MICROPROCESSORS**
- **USEFUL AS INPUT OR OUTPUT PORT FOR MICROPROCESSORS**
- **FUNCTIONALLY IDENTICAL TO 'LS573**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

**LOGIC SYMBOL**




VCC = Pin 20
GND = Pin 10

**ORDERING CODE:** See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE<br>VCC = +5.0 V ±5%,<br>TA = 0°C to +70°C | MILITARY GRADE<br>VCC = +5.0 V ±10%,<br>TA = -55°C to +125°C | PKG TYPE |
|---|---|---|---|---|
| Plastic DIP (P) | A | 74LS563PC | | 9Z |
| Ceramic DIP (D) | A | 74LS563DC | 54LS563DM | 4E |
| Flatpak (F) | A | 74LS563FC | 54LS563FM | 4F |

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PIN NAMES | DESCRIPTION | 54/74LS (U.L.)<br>HIGH/LOW |
|---|---|---|
| $D_0 - D_7$ | Data Inputs | 0.5/0.25 |
| LE | Latch Enable Input (Active HIGH) | 0.5/0.25 |
| $\overline{OE}$ | 3-State Output Enable Input (Active LOW) | 0.5/0.25 |
| $\overline{O}_0 - \overline{O}_7$ | 3-State Latch Outputs | 65/15<br>(25)/(7.5) |