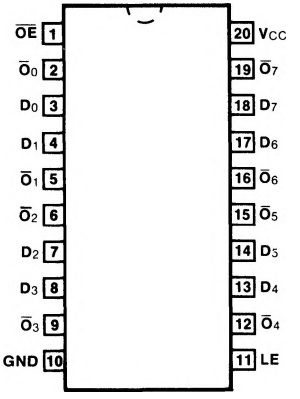
54LS/74LS533

OCTAL TRANSPARENT LATCH

(With 3-State Outputs)

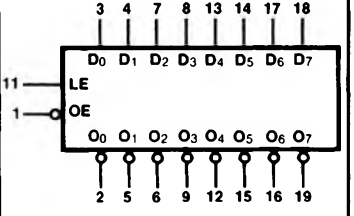
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '533 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state. The '533 is the same as the '373, except that the outputs are inverted. For detailed specifications please see the '373 data sheet, but note that the propagation delays from data to output are 5.0 ns longer for the 'LS533 than for the 'LS373.

- **EIGHT LATCHES IN A SINGLE PACKAGE**
- **3-STATE OUTPUTS FOR BUS INTERFACING**

LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V, ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS533PC		9Z
Ceramic DIP (D)	A	74LS533DC	54LS533DM	4E
Flatpak (F)	A	74LS533FC	54LS533FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
D0 — D7	Data Inputs	0.5/0.25
LE	Latch Enable Input (Active HIGH)	0.5/0.25
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.25
$\overline{O}_0$ — $\overline{O}_7$	Complementary 3-State Outputs	65/15 (25)/(7.5)