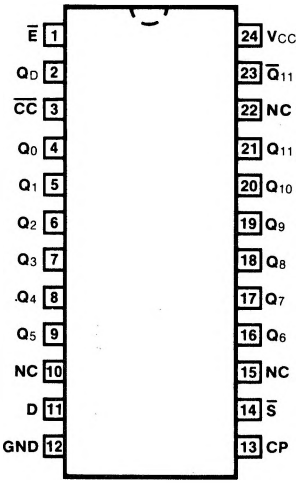
54LS/74LS504

12-BIT SUCCESSIVE APPROXIMATION REGISTER

(With Expansion Control)

CONNECTION DIAGRAM
PINOUT A



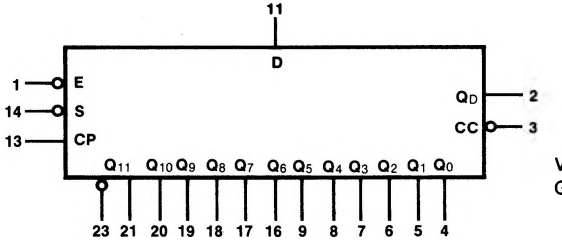
DESCRIPTION — The 'LS504 performs serial-to-parallel conversion and provides a Conversion Complete ($\overline{CC}$) signal. The 'LS504 is a 12-bit version of the 8-bit 'LS502 and has an active LOW Enable ($\overline{E}$) input for expansion, similar to the 'LS503. For detailed discussion of the various operations, please see the 'LS502 and 'LS503 data sheets.

- **PERFORMS SERIAL-TO-PARALLEL CONVERSION**
- **EXPANSION CONTROL FOR LONGER WORDS**
- **STORAGE AND CONTROL FOR SUCCESSIVE APPROXIMATION A TO D CONVERSION**
- **LOW POWER SCHOTTKY VERSION OF 2504**

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS504PC		9N
Ceramic DIP (D)	A	74LS504DC	54LS504DM	6N
Flatpak (F)	A	74LS504FC	54LS504FM	4M

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
D	Serial Data Input	0.5/0.25
$\overline{S}$	Start Input (Active LOW)	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$\overline{E}$	Conversion Enable Input (Active LOW)	0.5/0.25
Q_D	Synchronized Serial Data Output	10/5.0 (2.5)
$\overline{CC}$	Conversion Complete Output (Active LOW)	10/5.0 (2.5)
$Q_0 - Q_{11}$	Parallel Register Outputs	10/5.0 (2.5)
$\overline{Q}_{11}$	Complement of Q_{11} Output	10/5.0 (2.5)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		90	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	15		MHz	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n or $\overline{CC}$		38 28	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_7		19 24	ns	Figs. 3-1, 3-5 CP = 4.5, $\overline{S}$ = Gnd

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{S}$ to CP	16 16		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{S}$ to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW D to CP	8.0 8.0		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D to CP	10 10		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	20 46		ns	Fig. 3-8