54LS/74LS503

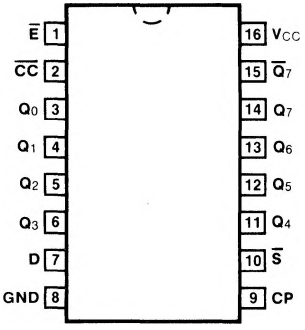
8-BIT SUCCESSIVE APPROXIMATION REGISTER

(With Expansion Control)

DESCRIPTION — The 'LS503 register is basically the same as the 'LS502 except that it has an active LOW Enable ($\overline{E}$) input that is used in cascading two or more packages for longer word lengths. A HIGH signal on $\overline{E}$, after a START operation, forces Q_7 HIGH and prevents the device from accepting serial data. With the $\overline{E}$ input of an 'LS503 connected to the $\overline{CC}$ output of a preceding (more significant) device, the 'LS503 will be inhibited until the preceding device is filled, causing its $\overline{CC}$ output to go LOW. This LOW signal then enables the 'LS503 to accept the serial data on subsequent clocks. For a description of the starting, shifting and conversion operations, please see the 'LS502 data sheet.

- **PERFORMS SERIAL-TO-PARALLEL CONVERSION**
- **EXPANSION CONTROL FOR LONGER WORDS**
- **STORAGE AND CONTROL FOR SUCCESSIVE APPROXIMATION A TO D CONVERSION**
- **LOW POWER SCHOTTKY VERSION OF 2503**

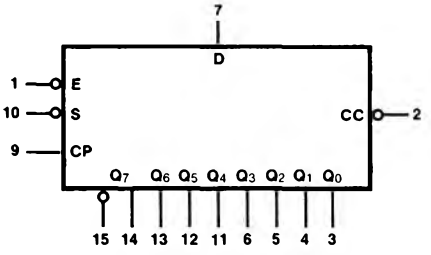
CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74LS503PC		9B
Ceramic DIP (D)	A	74LS503DC	54LS503DM	6B
Flatpak (F)	A	74LS503FC	54LS503FM	4L

LOGIC SYMBOL

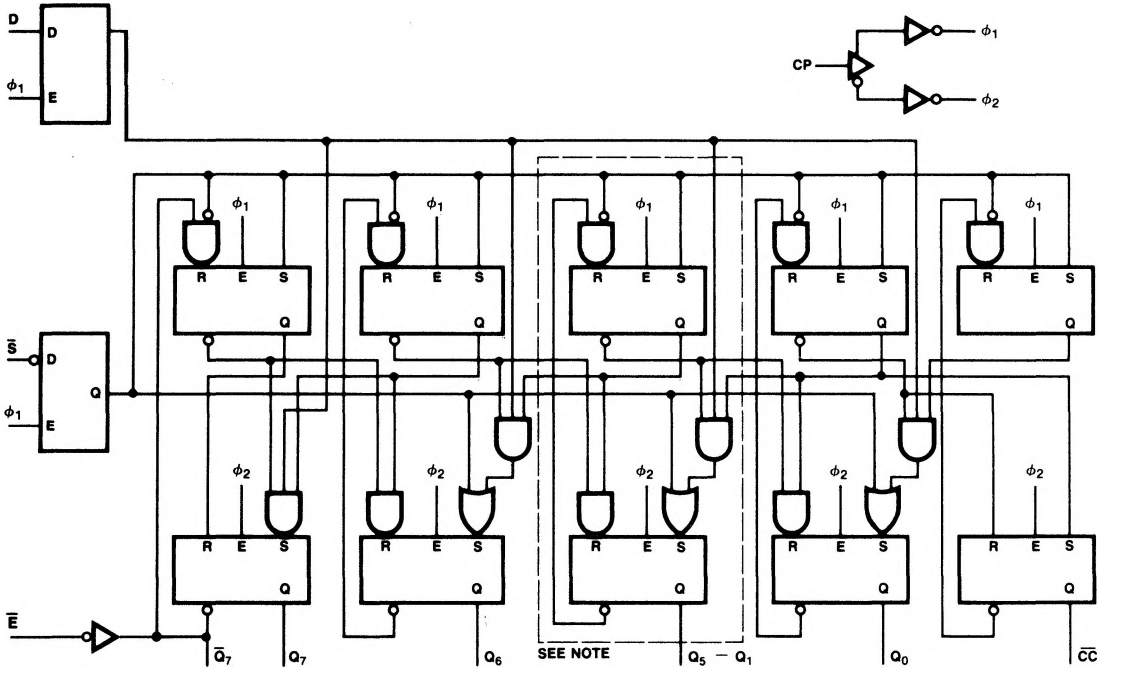


V_{CC} = Pin 16
GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

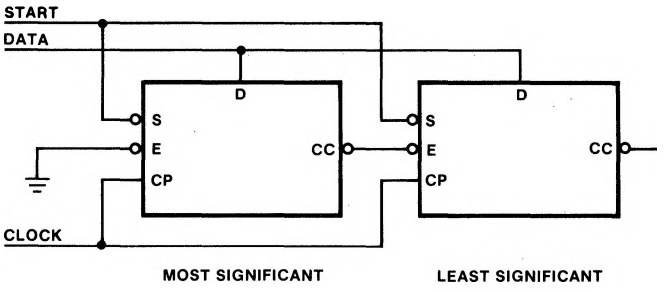
PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
D	Serial Data Input	0.5/0.25
$\overline{S}$	Start Input (Active LOW)	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$\overline{E}$	Conversion Enable Input (Active LOW)	10/5.0 (2.5)
$\overline{CC}$	Conversion Complete Output (Active LOW)	10/5.0 (2.5)
$Q_0 - Q_7$	Parallel Register Outputs	10/5.0 (2.5)
$\overline{Q}_7$	Complement of Q_7 Output	10/5.0 (2.5)

LOGIC DIAGRAM



Note: Cell logic is repeated for register stages Q_5 to Q_1.

CONNECTION FOR LONGER WORD LENGTHS



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		65	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	15		MHz	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n or $\overline{CC}$		38 28	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_7		19 24	ns	Figs. 3-1, 3-5 CP = 4.5 V, $\overline{S}$ = Gnd

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{S}$ to CP	16 16		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{S}$ to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW D to CP	8.0 8.0		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D to CP	10 10		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	20 46		ns	Fig. 3-8