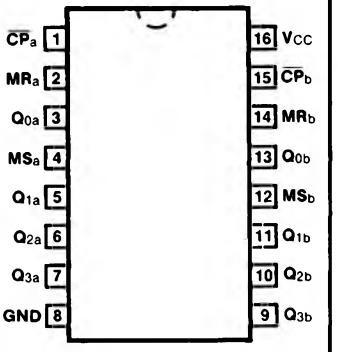
# 54LS/74LS490

## DUAL DECADE COUNTER

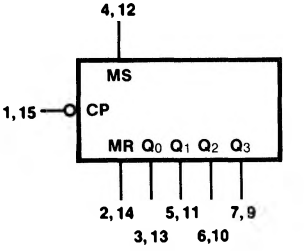
**DESCRIPTION** — The '490 contains a pair of high speed 4-stage ripple counters. Each half of the '490 has individual Clock, Master Reset and Master Set (Preset 9) inputs. Each section counts in the 8421 BCD code.

- **DUAL VERSION OF 54LS/74LS90**
- **INDIVIDUAL ASYNCHRONOUS CLEAR AND PRESET TO 9 FOR EACH COUNTER**
- **COUNT FREQUENCY — TYPICALLY 65 MHz**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **TTL AND CMOS COMPATIBLE**

**CONNECTION DIAGRAM**
PINOUT A




**LOGIC SYMBOL**




$V_{CC}$ = Pin 16
GND = Pin 8

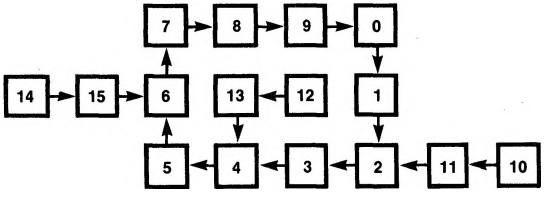
**ORDERING CODE:** See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE<br>$V_{CC}$ = +5.0 V ±5%, $T_A$ = 0°C to +70°C | MILITARY GRADE<br>$V_{CC}$ = +5.0 V ±10%, $T_A$ = -55°C to +125°C | PKG TYPE |
|---|---|---|---|---|
| Plastic DIP (P) | A | 74LS490PC | | 9B |
| Ceramic DIP (D) | A | 74LS490DC | 54LS490DM | 6B |
| Flatpak (F) | A | 74LS490FC | 54LS490FM | 4L |

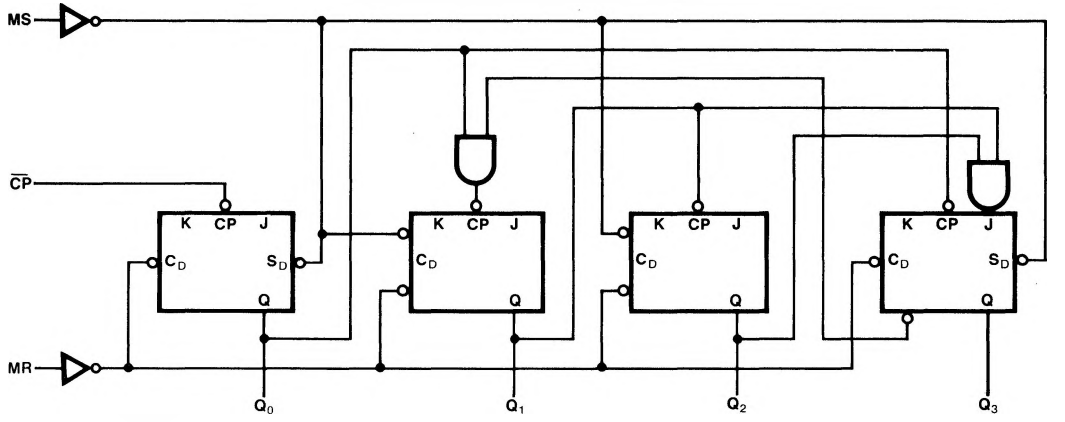
**INPUT LOADING/FAN-OUT:** See Section 3 for U.L definitions

| PIN NAMES | DESCRIPTION | 54/74LS (U.L.) HIGH/LOW |
|---|---|---|
| MS | Master Set (Set to 9) Input (Active HIGH) | 0.5/0.25 |
| MR | Master Reset Input (Active HIGH) | 0.5/0.25 |
| $\overline{CP}$ | Clock Pulse Input (Active Falling Edge) | 1.5/1.5 |
| $Q_0 - Q_3$ | Counter Outputs | 10/5.0<br>(2.5) |

**STATE DIAGRAM**



**LOGIC DIAGRAM** (one half shown)




**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| SYMBOL | PARAMETER | 54/74LS | | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $I_{CC}$ | Power Supply Current | | 26 | mA | $V_{CC}$ = Max |

**AC CHARACTERISTICS:** $V_{CC}$ = +5.0 V, $T_A$ = +25°C (See Section 3 for waveforms and load configurations)

| SYMBOL | PARAMETER | 54/74LS $C_L$ = 15 pF | | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $f_{max}$ | Maximum Count Frequency | 40 | | MHz | Figs. 3-1, 3-9 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$\overline{CP}$ to $Q_0$ | | 15<br>15 | ns | Figs. 3-1, 3-9 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$\overline{CP}$ to $Q_1$ or $Q_3$ | | 30<br>30 | ns | Figs. 3-1, 3-9 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$\overline{CP}$ to $Q_2$ | | 45<br>45 | ns | Figs. 3-1, 3-9 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>MS to $Q_n$ | | 35<br>35 | ns | Figs. 3-1, 3-17 |
| $t_{PHL}$ | Propagation Delay<br>MR to $Q_n$ | | 39 | ns | Figs. 3-1, 3-17 |

**AC OPERATING REQUIREMENTS:** $V_{CC}$ = +5.0 V, $T_A$ = +25°C

| SYMBOL | PARAMETER | 54/74LS | | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $t_w$ (H) | $\overline{CP}$ Pulse Width HIGH | 20 | | ns | Fig. 3-9 |
| $t_w$ (H) | MR, MS Pulse Width HIGH | 20 | | ns | Fig. 3-17 |
| $t_{rec}$ | Recovery Time, MR or MS to $\overline{CP}$ | 15 | | ns | Fig. 3-17 |