

54LS/74LS395

4-BIT SHIFT REGISTER (With 3-State Outputs)

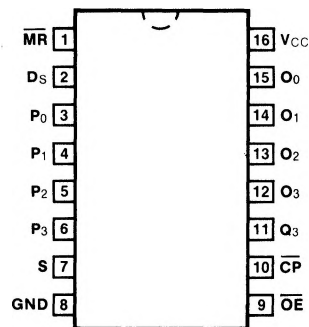
DESCRIPTION — The '395 is a 4-bit register with 3-state outputs and can operate in either a synchronous parallel load or a serial shift-right mode, as determined by the Select input. An asynchronous active LOW Master Reset (\overline{MR}) input overrides the synchronous operations and clears the register. An active LOW Output Enable (\overline{OE}) input controls the 3-state output buffers, but does not interfere with the other operations. The fourth stage also has a conventional output for linking purposes in multi-stage serial operations.

- SHIFT RIGHT OR PARALLEL 4-BIT REGISTER
- 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY CMOS AND TTL COMPATIBLE

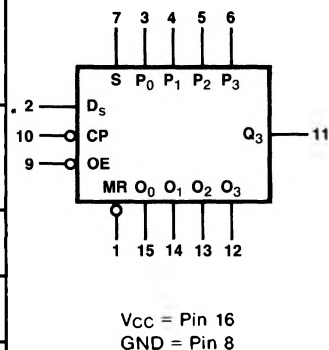
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0 \text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	74LS395PC		9B
Ceramic DIP (D)	A	74LS395DC	54LS395DM	6B
Flatpak (F)	A	74LS395FC	54LS395FM	4L

CONNECTION DIAGRAM PINOUT A



LOGIC SYMBOL



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$P_0 - P_3$	Parallel Data Inputs	0.5/0.25
D_S	Serial Data Input	0.5/0.25
S	Mode Select Input	0.5/0.25
\overline{CP}	Clock Pulse Input (Active Falling Edge)	0.5/0.25
\overline{MR}	Master Reset Input (Active LOW)	0.5/0.25
\overline{OE}	Output Enable Input (Active LOW)	0.5/0.25
$O_0 - O_3$	3-State Register Outputs	65/5.0 (25)/(2.5)
Q_3	Flip-flop Output	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '395 contains four D-type edge-triggered flip-flops and auxiliary gating to select a D input either from a Parallel (P_n) input or from the preceding stage. When the Select input is HIGH, the P_n inputs are enabled. A LOW signal on the S input enables the serial inputs for shift-right operations, as indicated in the Truth Table.

State changes are initiated by HIGH-to-LOW transitions on the Clock Pulse (\overline{CP}) input. Signals on the P_n , D_s and S inputs can change when the Clock is in either state, provided that the recommended setup and hold times are observed. When the S input is LOW, a \overline{CP} HIGH-LOW transition transfers data in Q_0 to Q_1 , Q_1 to Q_2 , and Q_2 to Q_3 . A left-shift is accomplished by connecting the outputs back to the P_n inputs, but offset one place to the left, i.e., Q_3 to P_2 , Q_2 to P_1 , and Q_1 to P_0 , with P_3 acting as the linking input from another package.

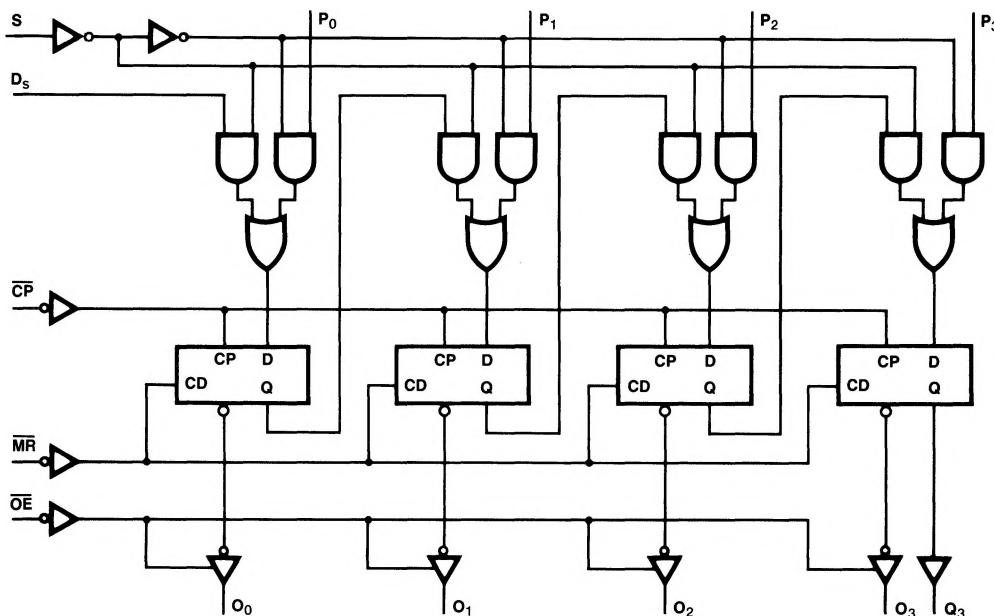
When the \overline{OE} input is HIGH, the output buffers are disabled and the $O_0 - O_3$ outputs are in a high impedance condition. The shifting, parallel loading or resetting operations can still be accomplished, however.

MODE SELECT TABLE

OPERATING MODE	INPUTS @ t_n					OUTPUTS @ t_{n+1}			
	\overline{MR}	\overline{CP}	S	D_s	P_n	O_0	O_1	O_2	O_3
Asynchronous Reset	L	X	X	X	X	L	L	L	L
Shift, SET First Stage	H	$\overline{1}$	L	H	X	H	O_{0n}	O_{1n}	O_{2n}
Shift, RESET First Stage	H	$\overline{1}$	L	L	X	L	O_{0n}	O_{1n}	O_{2n}
Parallel Load	H	$\overline{1}$	H	X	P_n	P_0	P_1	P_2	P_3

t_n, t_{n+1} = Time before and after CP HIGH-to-LOW transition
 H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74LS		UNITS	CONDITIONS
			Min	Max		
I_{OS}	Output Short Circuit Current		-20	-100	mA	$V_{CC} = \text{Max}$
I_{CC}	Power Supply Current	Output OFF		29	mA	$V_{CC} = \text{Max}; P_n = \text{Gnd}$ $\overline{CP} = \text{L}$ $\overline{OE}, D_S, S = 4.5 \text{ V}$
		Outputs ON		25		$V_{CC} = \text{Max}; D_S, S = 4.5 \text{ V}$ $\overline{OE}, \overline{CP}, P_n = \text{Gnd}$

AC CHARACTERISTICS: $V_{CC} = +5.0 \text{ V}$, $T_A = +25^\circ \text{C}$ (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER		54/74LS		UNITS	CONDITIONS
			$C_L = 15 \text{ pF}$			
			Min	Max		
f_{max}	Maximum Shift Frequency		30		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay \overline{CP} to O_n			35 25	ns	Figs. 3-1, 3-9
t_{PHL}	Propagation Delay \overline{MR} to O_n			35	ns	Figs. 3-1, 3-17
t_{PZH} t_{PZL}	Output Enable Time			20 20	ns	Figs. 3-3, 3-11, 3-12 $R_L = 2 \text{ k}\Omega$
t_{PHZ} t_{PLZ}	Output Disable Time			17 23	ns	Figs. 3-3, 3-11, 3-12 $R_L = 2 \text{ k}\Omega$ $C_L = 5 \text{ pF}$

AC OPERATING REQUIREMENTS: $V_{CC} = +5.0 \text{ V}$, $T_A = +25^\circ \text{C}$

SYMBOL	PARAMETER		54/74LS		UNITS	CONDITIONS
			Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW S, D_S or P_n to \overline{CP}		20		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time HIGH or LOW S, D_S or P_n to \overline{CP}		5.0		ns	Fig. 3-7
t_w (L)	\overline{CP} Pulse Width LOW		18		ns	Fig. 3-9
t_w (L)	\overline{MR} Pulse Width LOW		20		ns	Fig. 3-17