54LS/74LS393

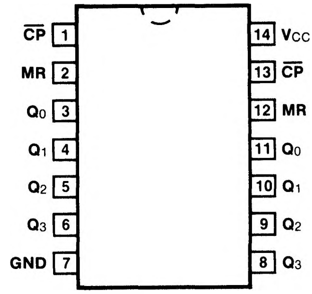
DUAL MODULO-16 COUNTER

DESCRIPTION — The '393 contains a pair of high speed 4-stage ripple counters. Each half of the '393 operates as a modulo-16 binary divider, with the last three stages triggered in a ripple fashion. The flip-flops are triggered by a HIGH-to-LOW transition of their $\overline{CP}$ inputs. Each half of each circuit type has a Master Reset input which responds to a HIGH signal by forcing all four outputs to the LOW state. For detail specifications, please refer to the '390 data sheet.

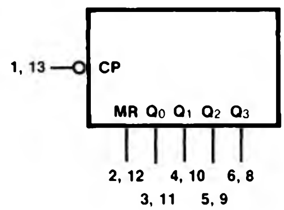
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74LS393PC		9A
Ceramic DIP (D)	A	74LS393DC	54LS393DM	6A
Flatpak (F)	A	74LS393FC	54LS393FM	3I

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL
(each half)



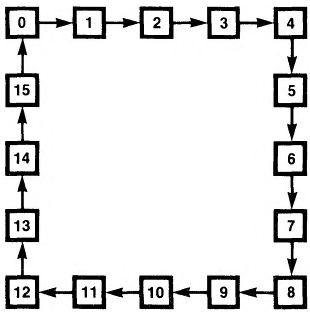
V_{CC} = Pin 14
GND = Pin 7

INPUT LOADING/FAN-OUT: See Section 3 for U.L definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	1.0/1.5
MR	Asynchronous Master Reset Input (Active HIGH)	0.5/0.25
Q_0 — Q_3	Flip-flop Outputs	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — Each half of the '393 operates in the modulo-16 binary sequence, as indicated in the ÷16 Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the $\overline{CP}$ input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs do not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting.

STATE DIAGRAM



TRUTH TABLE

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM (one half shown)