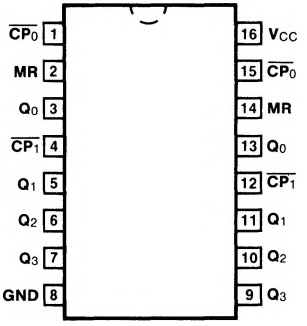
54LS/74LS390

DUAL DECADE COUNTER

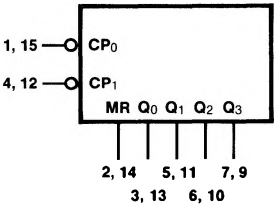
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '390 contains a pair of high speed 4-stage ripple counters. Each half of the '390 is partitioned into a divide-by-two section and a divide-by-five section, with a separate clock input for each section. The two sections can be connected to count in the 8421 BCD code or they can count in a bi-quinary sequence to provide a square wave (50% duty cycle) at the final output.

Each half of the '390 contains a ÷5 section that is independent except for the common MR function. The ÷5 section operates in 421 binary sequence, as shown in the ÷5 Truth Table, with the third stage output exhibiting a 20% duty cycle when the input frequency is constant. To obtain a ÷10 function having a 50% duty cycle output, connect the input signal to $\overline{CP_1}$ and connect the Q_3 output to the $\overline{CP_0}$ input; the Q_0 output provides the desired 50% duty cycle output. If the input frequency is connected to $\overline{CP_0}$ and the Q_0 output is connected to $\overline{CP_1}$, a decade divider operating in the 8421 BCD code is obtained, as shown in the BCD Truth Table. Since the flip-flops change state asynchronously, logic signals derived from combinations of '390 outputs are also subject to decoding spikes. A HIGH signal on MR forces all outputs LOW and prevents counting.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

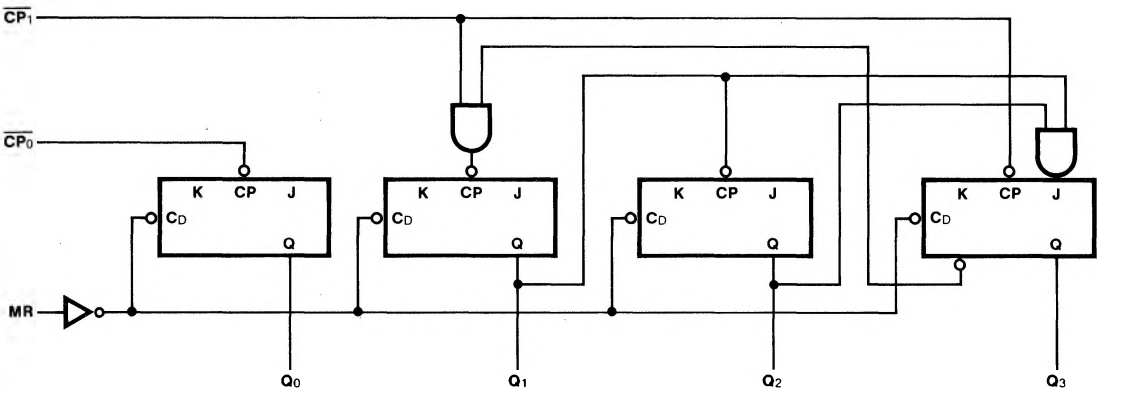
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS390PC		9B
Ceramic DIP (D)	A	74LS390DC	54LS390DM	6B
Flatpak (F)	A	74LS390FC	54LS390FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$\overline{CP_0}$	÷2 Section Clock Input (Active Falling Edge)	1.0/1.5
$\overline{CP_1}$	÷5 Section Clock Input (Active Falling Edge)	2.0/2.0
MR	Asynchronous Master Reset Input (Active HIGH)	0.5/0.25
Q_0 — Q_3	Flip-flop Outputs*	10/5.0 (2.5)

*The Q_0 Output is guaranteed to drive the full rated fan-out plus the $\overline{CP_1}$ input.

LOGIC DIAGRAM (one half shown)



BCD TRUTH TABLE
(Input on $\overline{CP_0}$; Q_0 to $\overline{CP_1}$)

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

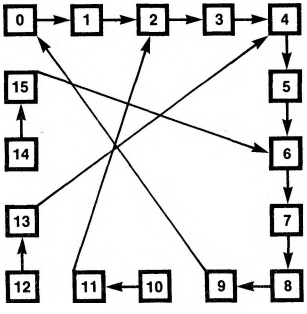
H = HIGH Voltage Level
L = LOW Voltage Level

÷5 TRUTH TABLE
(Input on $\overline{CP_1}$)

COUNT	OUTPUTS		
	Q_3	Q_2	Q_1
0	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level

STATE DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{IH}	Input HIGH Current, $\overline{CP}_0$, $\overline{CP}_1$			0.1	mA	V_{CC} = Max, V_{IN} = 5.5 V
I_{CC}	Power Supply Current	'390		30	mA	V_{CC} = Max
		'393				

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF Min	54/74LS C_L = 15 pF Max	UNITS	CONDITIONS
f_{max}	Maximum Count Frequency $\overline{CP}_0$ ('390) or $\overline{CP}$ ('393)	40		MHz	Figs. 3-1, 3-9
f_{max}	$\overline{CP}_1$ Maximum Count Frequency	20		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_0$ ('390) or $\overline{CP}$ ('393) to Q_0		15 15	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_1$ ('390) to Q_1		21 21	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_1$ ('390) to Q_2		30 30	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_1$ ('390) to Q_3		21 21	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ ('393) to Q_1		30 30	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ ('393) to Q_2		40 40	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ ('393) to Q_3		54 54	ns	Figs. 3-1, 3-9
t_{PHL}	Propagation Delay MR to Q_n		35	ns	Figs. 3-1, 3-17

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_w (L)	CP or CP_0 Pulse Width LOW	12		ns	Fig. 3-9
t_w (L)	CP_1 Pulse Width LOW	25		ns	Fig. 3-9
t_w (H)	MR Pulse Width HIGH	20		ns	Fig. 3-17
t_{rec}	Recovery Time MR to CP	15		ns	Fig. 3-17