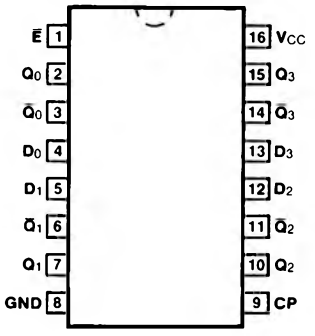
54LS/74LS379

QUAD PARALLEL REGISTER

(With Enable)

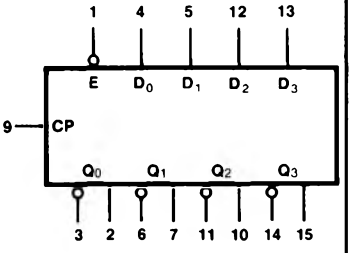
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '379 is a 4-bit register with buffered common Enable. This device is similar to the '175 but features the common Enable rather than common Master Reset.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **BUFFERED COMMON ENABLE INPUT**
- **TRUE AND COMPLEMENT OUTPUTS**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS379PC		9B
Ceramic DIP (D)	A	74LS379DC	54LS379DM	6B
Flatpak (F)	A	74LS379FC	54LS379FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$\overline{E}$	Enable Input (Active LOW)	0.5/0.25
D_0 — D_3	Data Inputs	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
Q_0 — Q_3	Flip-flop Outputs	10/5.0 (2.5)
$\overline{Q}_0$ — $\overline{Q}_3$	Complement Outputs	10/5.0 (2.5)

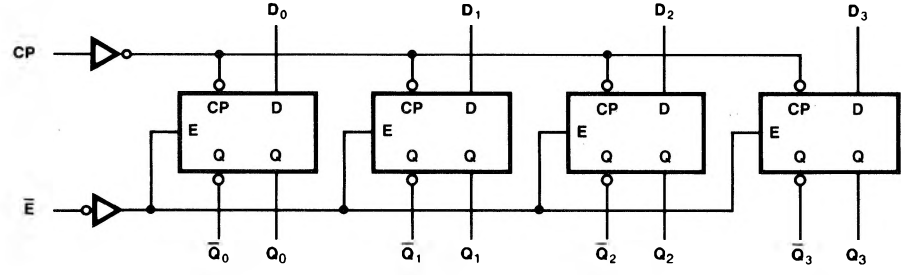
FUNCTIONAL DESCRIPTION — The '379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops. When the $\overline{E}$ input is HIGH, the register will retain the present data independent of the CP input. The D_n and $\overline{E}$ inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed.

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	⌐	X	No Change	No Change
L	⌐	H	H	L
L	⌐	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		18	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		C_L = 15 pF			
		Min	Max		
f_{max}	Maximum Clock Frequency	30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		27 27	ns	

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to CP	20 20		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to CP	5.0 5.0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{E}$ to CP	25 25		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{E}$ to CP	5.0 5.0		ns	
t_w (L)	CP Pulse Width LOW	17		ns	Fig. 3-8