

54LS/74LS373

OCTAL TRANSPARENT LATCH (With 3-State Outputs)

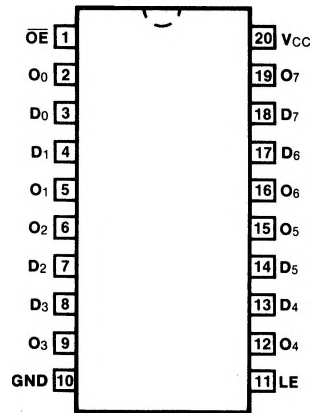
DESCRIPTION — The '373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedance state.

- EIGHT LATCHES IN A SINGLE PACKAGE
- 3-STATE OUTPUTS FOR BUS INTERFACING

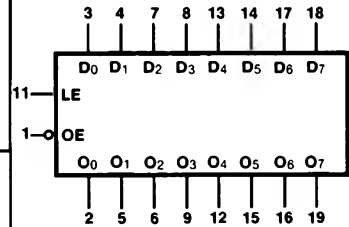
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	74LS373PC		9Z
Ceramic DIP (D)	A	74LS373DC	54LS373DM	4E
Flatpak (F)	A	74LS373FC	54LS373FM	4F

CONNECTION DIAGRAM PINOUT A



LOGIC SYMBOL



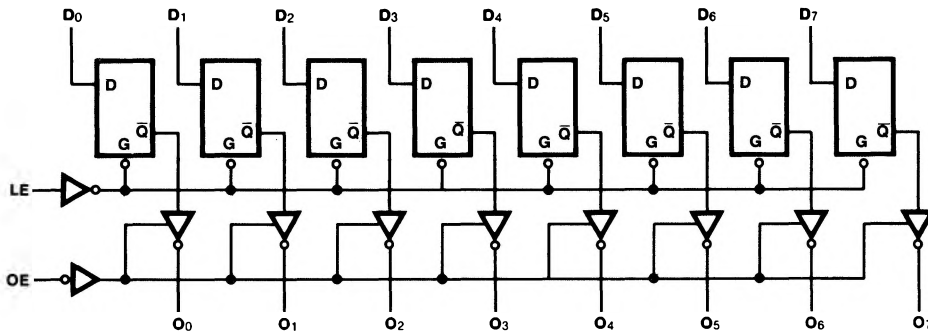
$V_{CC} = \text{Pin } 20$
 $GND = \text{Pin } 10$

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$D_0 - D_7$	Data Inputs	0.5/0.25
LE	Latch Enable Input (Active HIGH)	0.5/0.25
OE	Output Enable Input (Active LOW)	0.5/0.25
$O_0 - O_7$	3-State Latch Outputs	65/15 (25)/(7.5)

FUNCTIONAL DESCRIPTION — The '373 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are in the bi-state mode. When \overline{OE} is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74LS		UNITS	CONDITIONS
			Min	Max		
I _{CC}	Power Supply Current	Outputs OFF		40	mA	V _{CC} = Max, \overline{OE} = 4.5 V D _n , LE = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER		54/74LS		UNITS	CONDITIONS
			C _L = 50 pF			
			Min	Max		
t _{PLH} t _{PHL}	Propagation Delay D _n to O _n		18 20		ns	Figs. 3-1, 3-5
t _{PLH} t _{PHL}	Propagation Delay LE to O _n		30 30		ns	Figs. 3-1, 3-8
t _{PZH} t _{PZL}	Output Enable Time		28 36		ns	Figs. 3-3, 3-11, 3-12 R _L = 667Ω
t _{PHZ} t _{PLZ}	Output Disable Time		20 25		ns	Figs. 3-3, 3-11, 3-12 R _L = 667Ω, C _L = 5.0 pF

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER		54/74LS		UNITS	CONDITIONS
			Min	Max		
t _s (H) t _s (L)	Setup Time HIGH or LOW D _n to LE		0 0		ns	Fig. 3-14
t _h (H) t _h (L)	Hold Time HIGH or LOW D _n to LE		10 10		ns	
t _w (H) t _w (L)	LE Pulse Width HIGH or LOW		15 15		ns	Fig. 3-8