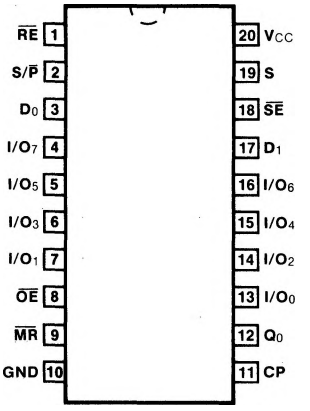
54LS/74LS322

8-BIT SERIAL/PARALLEL REGISTER

(With Sign Extend)

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '322 is an 8-bit shift register with provision for either serial or parallel loading and with 3-state parallel outputs plus a bi-state serial output. Parallel data inputs and parallel outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with sign extend and parallel load. An asynchronous Master Reset ($\overline{MR}$) input overrides clocked operation and clears the register. The '322 is specifically designed for operation with the '384 Multiplier and provides the sign extend function required for the '384.

ORDERING CODE: See Section 9

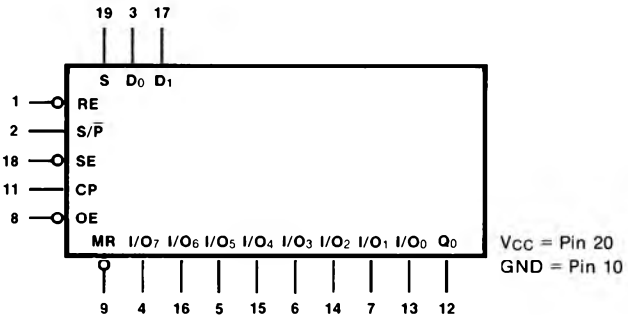
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS322PC		9Z
Ceramic DIP (D)	A	74LS322DC	54LS322DM	4E
Flatpak (F)	A	74LS322FC	54LS322FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

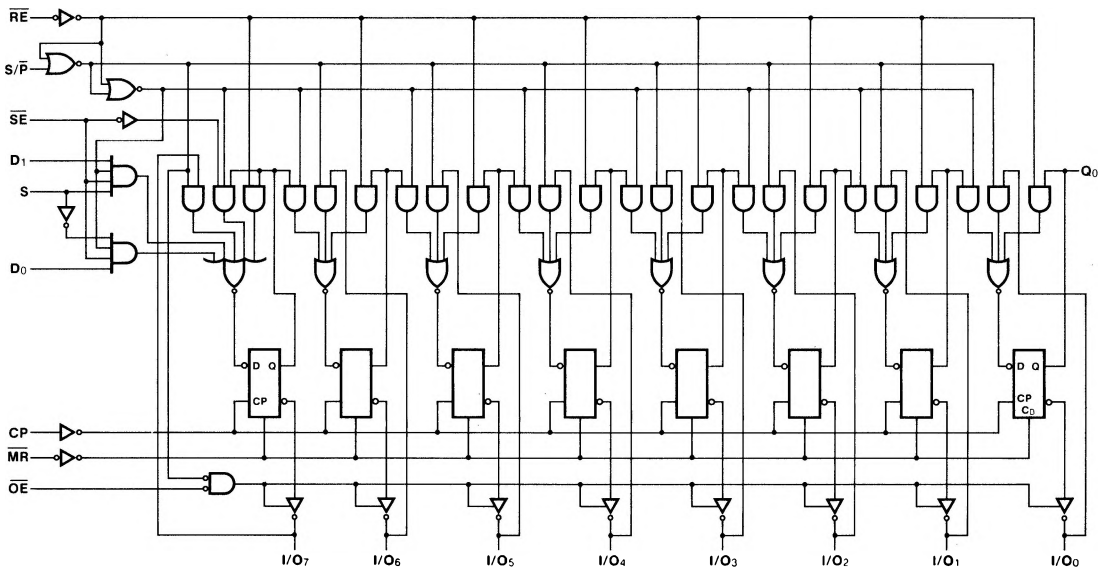
PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$\overline{RE}$	Register Enable Input (Active LOW)	0.5/0.23
S/$\overline{P}$	Serial (HIGH) or Parallel (LOW) Mode Control Input	0.5/0.23
$\overline{SE}$	Sign Extend Input (Active LOW)	1.5/0.68
S	Serial Data Select Input	1.0/0.45
D_0, D_1	Serial Data Inputs	0.5/0.23
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.23
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	0.5/0.23
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.23
Q_0	Bi-State Serial Output	11/5.0 (2.5)
I/O_0 — I/O_7	Multiplexed Parallel Inputs or 3-State Parallel Outputs	0.5/0.23 65/5.0 (25)/(2.5)

FUNCTIONAL DESCRIPTION — The '322 contains eight D-type edge triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A LOW signal on $\overline{RE}$ enables shifting or parallel loading, while a HIGH signal enables the hold mode. A HIGH signal on S/$\overline{P}$ enables shift right, while a LOW signal disables the 3-state output buffers and enables parallel loading. In the shift right mode a HIGH signal on $\overline{SE}$ enables serial entry from either D_0 or D_1, as determined by the S input. A LOW signal on $\overline{SE}$ enables shift right but Q_7 reloads its contents, thus performing the sign extend function required for the '384 Twos Complement Multiplier. A HIGH signal on $\overline{OE}$ disables the 3-state output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

LOGIC SYMBOL



LOGIC DIAGRAM



MODE TABLE

MODE	INPUTS							OUTPUTS								
	$\overline{MR}$	$\overline{RE}$	S/$\overline{P}$	$\overline{SE}$	S	$\overline{OE}$*	CP	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Q_0
Clear	L	X	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	X	X	X	X	H	X	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel Load	H	L	L	X	X	X	⎍	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	I_0
Shift Right	H	L	H	H	L	L	⎍	D_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
	H	L	H	H	H	L	⎍	D_1	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
Sign Extend	H	L	H	L	X	L	⎍	O_7	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
Hold	H	H	X	X	X	L	⎍	NC	NC	NC	NC	NC	NC	NC	NC	NC

*When the $\overline{OE}$ input is HIGH, all I/O_n terminals are at the high-impedance state; sequential operation or clearing of the register is not affected.
1. I_7 — I_0 = The level of the steady-state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q_0) are isolated from the I/O terminal.
2. D_0, D_1 = The level of the steady-state inputs to the serial multiplexer input.
3. O_7 — O_0 = The level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.

NC = No Change Z = High-Impedance Output State H = HIGH Voltage Level L = LOW Voltage Level

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		60	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	35		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n		23 25	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0		25 29	ns	Figs. 3-1, 3-16
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n		33	ns	Figs. 3-1, 3-16
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0		30	ns	Figs. 3-1, 3-16
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n		18 23	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n		15 15	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ, C_L = 5 pF
t_{PZH} t_{PZL}	Output Enable Time S/$\overline{P}$ to I/O_n		25 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ
t_{PHZ} t_{PLZ}	Output Disable Time S/$\overline{P}$ to I/O_n		23 23	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ, C_L = 5 pF

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{RE}$ to CP	24 24		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{RE}$ to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW D_0, D_1 or I/O_n to CP	10 10		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW D_0, D_1 or I/O_n to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{SE}$ to CP	15 15		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{SE}$ to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW S/$\overline{P}$ to CP	24 24		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW S to CP	15 15		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW S or S/$\overline{P}$ to CP	0 0		ns	
t_w (H)	CP Pulse Width HIGH	15		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	15		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	15		ns	