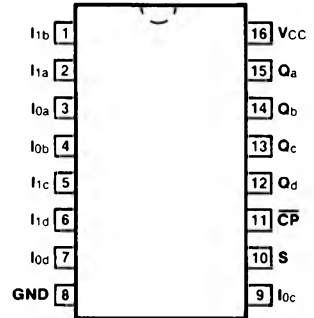


54/74298 54LS/74LS298

QUAD 2-PORT REGISTER (Multiplexer with Storage)

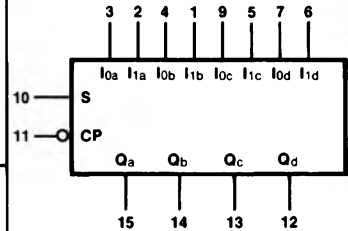
**CONNECTION DIAGRAM
PINOUT A**



DESCRIPTION — The '298 is a quad 2-port register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register synchronous with the HIGH-to-LOW transition of the Clock input.

- **SELECT FROM TWO DATA SOURCES**
- **FULLY EDGE-TRIGGERED OPERATION**
- **TYPICAL POWER DISSIPATION OF 65 mW (LS298)**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	A	74298PC, 74LS298PC		9B
Ceramic DIP (D)	A	74298DC, 74LS298DC	54298DM, 54LS298DM	6B
Flatpak (F)	A	74298FC, 74LS298FC	54298FM, 54LS298FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
S	Common Select Input	1.0/1.0	0.5/0.25
CP	Clock Pulse Input (Active Falling Edge)	1.0/1.0	0.5/0.25
I0a — I0d	Source 0 Data Inputs	1.0/1.0	0.5/0.25
I1a — I1d	Source 1 Data Inputs	1.0/1.0	0.5/0.25
Qa — Qd	Flip-flop Outputs	20/10	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — This device is a high speed quad 2-port register. It selects four bits of data from two sources (ports) under the control of a Common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input (\overline{CP}). The 4-bit output register is fully edge-triggered. The Data inputs (I_{nx}) and Select input (S) need be stable only one setup time prior to the HIGH-to-LOW transition of the clock for predictable operation.

TRUTH TABLE

INPUTS			OUTPUT
S	I_{0x}	I_{1x}	Q_x
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

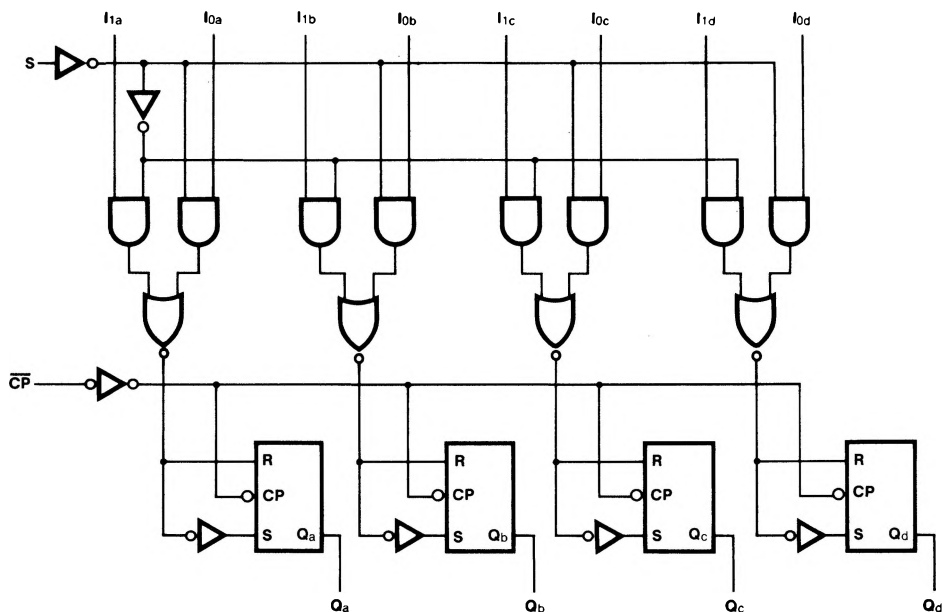
l = LOW Voltage Level one setup time prior to the HIGH-to-LOW clock transition.

h = HIGH Voltage Level one setup time prior to the HIGH-to-LOW clock transition.

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

LOGIC DIAGRAM

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max				
I _{CC}	Power Supply Current	65		21		mA	I _{0n} , I _{1n} , S = Gnd $\overline{CP} = \text{L}, V_{CC} = \text{Max}$

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		C _L = 15 pF R _L = 400 Ω		C _L = 15 pF			
		Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation Delay CP to Q _n	27 32		25 25		ns	Figs. 3-1, 3-9

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t _s (H) t _s (L)	Setup Time HIGH or LOW S to \overline{CP}	25 25		25 25		ns	Fig. 3-7
t _h (H) t _h (L)	Hold Time HIGH or LOW S to \overline{CP}	0 0		0 0		ns	
t _s (H) t _s (L)	Setup Time HIGH or LOW I _{0x} or I _{1x} to \overline{CP}	15 15		15 15		ns	
t _h (H) t _h (L)	Hold Time HIGH or LOW I _{0x} or I _{1x} to \overline{CP}	5.0 5.0		5.0 5.0		ns	
t _w (H) t _w (L)	\overline{CP} Pulse Width HIGH or LOW	20 20		20 20		ns	Fig. 3-9