54LS/74LS295A

4-BIT SHIFT REGISTER

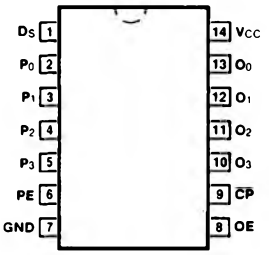
(With 3-State Outputs)

DESCRIPTION — The '295A is a 4-bit shift register with serial and parallel synchronous operating modes, and independent 3-state output buffers. The Parallel Enable input (PE) controls the shift-right or parallel load operation. All data transfers and shifting occur synchronous with the HIGH-to-LOW clock transition.

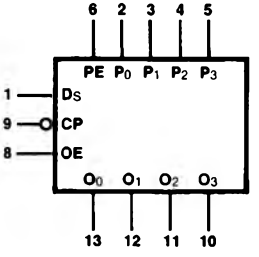
The 3-state output buffers are controlled by an active HIGH Output Enable input (OE). Disabling the output buffers does not affect the shifting or loading of input data, but it does inhibit serial expansion. The device is fabricated with the Schottky barrier diode process for high speed.

- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**
- **NEGATIVE EDGE-TRIGGERED CLOCK INPUT**
- **PARALLEL ENABLE MODE CONTROL INPUT**
- **3-STATE BUSSABLE OUTPUT BUFFERS**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0° C to +70° C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	74LS295APC		9A
Ceramic DIP (D)	A	74LS295ADC	54LS295ADM	6A
Flatpak (F)	A	74LS295AFC	54LS295AFM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
PE	Parallel Enable Input (Active HIGH)	0.5/0.25
DS	Serial Data Input	0.5/0.25
P0 — P3	Parallel Data Inputs	0.5/0.25
OE	3-State Output Enable Input (Active HIGH)	0.5/0.25
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	0.5/0.25
O0 — O3	3-State Outputs	65/5.0 (25)/(2.5)

FUNCTIONAL DESCRIPTION — This device is a 4-bit shift register with serial and parallel synchronous operating modes. It has a Serial Data (D_S) and four Parallel Data (P_0 — P_3) inputs and four parallel 3-State output buffers (O_0 — O_3). When the Parallel Enable (PE) input is HIGH, data is transferred from the Parallel Data inputs (P_0 — P_3) into the register synchronous with the HIGH-to-LOW transition of the Clock ($\overline{CP}$). When the PE is LOW, a HIGH-to-LOW transition on the clock transfers the serial data on the D_S input to register Q_0, and shifts data from Q_0 to Q_1, Q_1 to Q_2 and Q_2 to Q_3. The input data and parallel enable are fully edged-triggered and must be stable only one setup time before the HIGH-to-LOW clock transition.

The 3-state output buffers are controlled by an active HIGH Output Enable input (OE). When the OE is HIGH, the four register outputs appear at the O_0 — O_3 outputs. When OE is LOW, the outputs are forced to a high impedance OFF state. The 3-state output buffers are completely independent of the register operation, i.e., the input transitions on the OE input do not affect the serial or parallel data transfers of the register. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

MODE SELECT TABLE

OPERATING MODE	INPUTS				OUTPUTS			
	PE	$\overline{CP}$	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift Right	l	⌐L	l	X	L	q_0	q_1	q_2
	l	⌐L	h	X	H	q_0	q_1	q_2
Parallel Load	h	⌐L	X	p_n	p_0	p_1	p_2	p_3

*The indicated data appears at the Q outputs when OE is HIGH. When OE is LOW, the indicated data is loaded into the register, but the outputs are all forced to the high impedance OFF state.

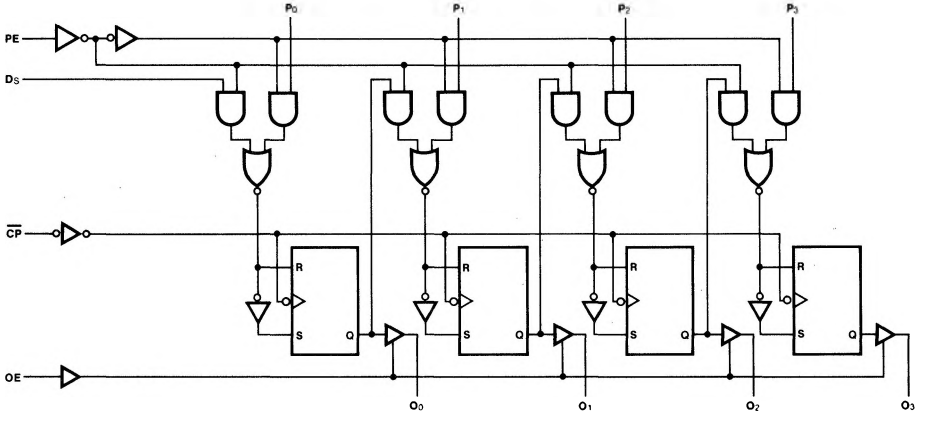
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.

l = LOW Voltage Level one set-up time prior to the HIGH-to-LOW clock transition

h = HIGH Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Curent		-20	-100	mA	V_{CC} = Max
I_{CC}	Power Supply Current	Outputs ON		23	mA	V_{CC} = Max, P_n = Gnd PE, D_S, OE = 4.5 V $\overline{CP}$ = ⊓_
		Outputs OFF		25		V_{CC} = Max, PE, D_S = 4.5 V P_n, OE, $\overline{CP}$ = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF Min	54/74LS C_L = 15 pF Max	UNITS	CONDITIONS
f_{max}	Maximum Shift Frequency	30		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_n		30 26	ns	Figs. 3-1, 3-9
t_{PZH} t_{PZL}	Output Enable Time		18 20	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ,
t_{PHZ} t_{PLZ}	Output Disable Time		24 20	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ, C_L = 5 pF

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW D_S , P_n to $\overline{CP}$	20 20		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time HIGH or LOW D_S, P_n to $\overline{CP}$	10 10		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW PE to $\overline{CP}$	20 20		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time HIGH or LOW PE to $\overline{CP}$	0 0		ns	
t_w (L)	$\overline{CP}$ Pulse Width LOW	20		ns	Fig. 3-9