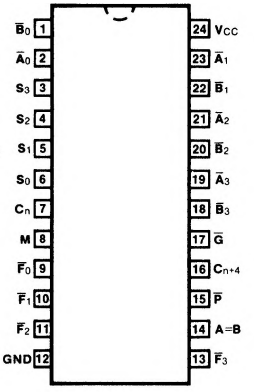
54LS/74LS181

4-BIT ARITHMETIC LOGIC UNIT

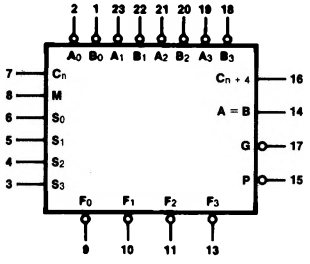
DESCRIPTION — The '181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations. For improved TTL, S-TTL and LP-TTL versions, please see the 9341 data sheet.

- **PROVIDES 16 ARITHMETIC OPERATIONS**
  ADD, SUBTRACT, COMPARE, DOUBLE, PLUS
  TWELVE OTHER ARITHMETIC OPERATIONS
- **PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES**
  EXCLUSIVE-OR, COMPARE, AND, NAND, OR, NOR,
  PLUS TEN OTHER LOGIC OPERATIONS
- **FULL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION ON LONG WORDS**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS181PC		9N
Ceramic DIP (D)	A	74LS181DC	54LS181DM	6N
Flatpak (F)	A	74LS181FC	54LS181FM	4M

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$\overline{A}_0$ — $\overline{A}_3$	Operand Inputs (Active LOW)	1.5/0.75
$\overline{B}_0$ — $\overline{B}_3$	Operand Inputs (Active LOW)	1.5/0.75
S_0 — S_3	Function Select Inputs	2.0/1.0
M	Mode Control Input	0.5/0.25
C_n	Carry Input	2.5/1.25
$\overline{F}_0$ — $\overline{F}_3$	Function Outputs (Active LOW)	10/5.0 (2.5)
A = B	Comparator Output	OC*/5.0 (2.5)
$\overline{G}$	Carry Generate Output (Active LOW)	10/10
$\overline{P}$	Carry Propagate Output (Active LOW)	10/5.0
C_{n+4}	Carry Output	10/5.0 (2.5)

*OC — Open Collector

FUNCTIONAL DESCRIPTION — The 'LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0 — S_3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). In the ADD mode, $\overline{P}$ indicates that $\overline{F}$ is 15 or more, while $\overline{G}$ indicates that $\overline{F}$ is 16 or more. In the SUBTRACT mode, $\overline{P}$ indicates that $\overline{F}$ is zero or less, while $\overline{G}$ indicates that $\overline{F}$ is less than zero. $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high speed operation the device is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of four 'LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open-collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

FUNCTION TABLE

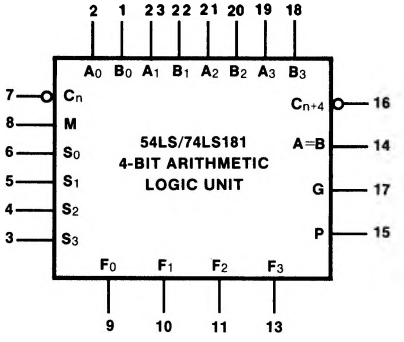
MODE SELECT INPUTS				ACTIVE LOW OPERANDS & F_n OUTPUTS		ACTIVE HIGH OPERANDS & F_n OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A + B
L	L	H	L	$\overline{A+B}$	A$\overline{B}$ minus 1	$\overline{A}B$	A + $\overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A+B}$	A plus (A + $\overline{B}$)	$\overline{AB}$	A plus A$\overline{B}$
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)	$\overline{B}$	(A + B) plus A$\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	A $\oplus$ B	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$	A$\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}B$	A plus (A + B)	$\overline{A+B}$	A plus AB
H	L	L	H	A $\oplus$ B	A plus B	A $\oplus$ B	A plus B
H	L	H	L	B	A$\overline{B}$ plus (A + B)	B	(A + $\overline{B}$) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A*	Logic 1	A plus A*
H	H	L	H	A$\overline{B}$	AB plus A	A + $\overline{B}$	(A + B) plus A
H	H	H	L	AB	A$\overline{B}$ minus A	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A	A	A minus 1

*each bit is shifted to the next more significant position

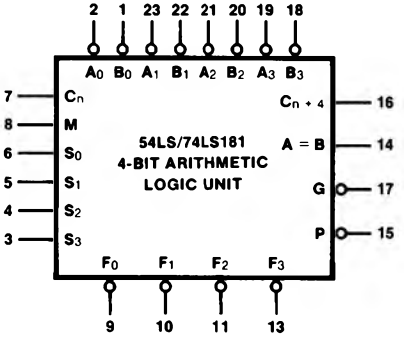
**arithmetic operations expressed in 2s complement notation

LOGIC SYMBOLS

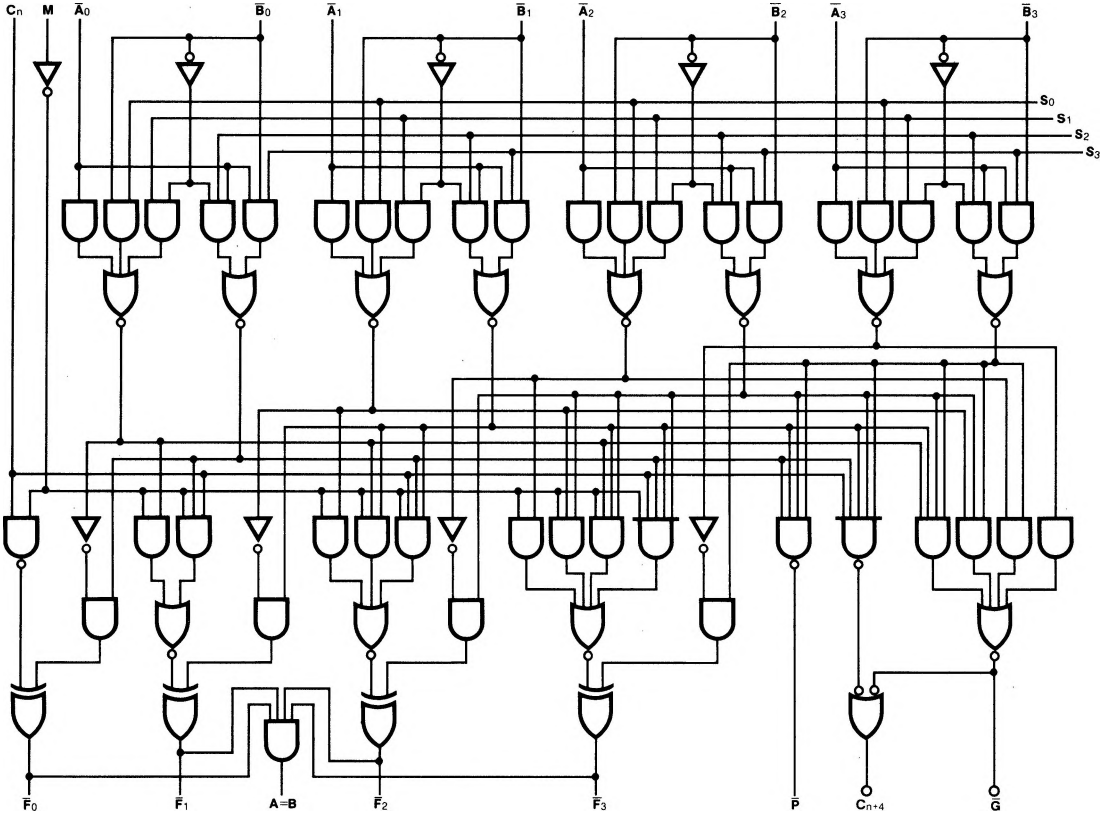
ACTIVE HIGH OPERANDS



ACTIVE LOW OPERANDS



LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OH}	Output HIGH Current, A = B			100	μA	V_{CC} = Min, V_{OH} = 5.5 V
I_{CC}	Power Supply Current	XM		32	mA	V_{CC} = Max $\overline{B}_n$, C_n = Gnd S_n, M, $\overline{A}_n$ = 4.5 V
		XC		34		
		XM		35	mA	V_{CC} = Max $\overline{A}_n$, $\overline{B}_n$, C_n = Gnd M, S_n = 4.5 V
		XC		37		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF Min	54/74LS C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+4}		27 20	ns	M = Gnd, Figs. 3-1, 3-5 Tables I & II
t_{PLH} t_{PHL}	Propagation Delay C_n to $\overline{F}$		26 20	ns	M = Gnd, Figs. 3-1, 3-5 Table I
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$		29 23	ns	M, S_1, S_2 = Gnd; S_1, S_3 = 4.5 V; Figs. 3-1, 3-5 Table I
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$		32 26	ns	M, S_0, S_3 = Gnd; S_1, S_2 = 4.5 V; Figs. 3-1, 3-4, 3-5; Table II
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$		30 30	ns	M, S_1, S_2 = Gnd; S_0, S_3 = 4.5 V; Figs. 3-1, 3-4; Table I
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$		30 33	ns	M, S_0, S_3 = Gnd; S_1, S_2 = 4.5 V; Figs. 3-1, 3-4, 3-5; Table II
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$		32 25	ns	M, S_1, S_2 = Gnd; S_0, S_3 = 4.5 V; Figs. 3-1, 3-5: Table I
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$		32 32	ns	M, S_0, S_3 = Gnd; S_1, S_2 = 4.5 V; Figs. 3-1, 3-4, 3-5; Table II
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F}$		33 29	ns	M = 4.5 V; Figs. 3-1, 3-5; Table III
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to C_{n+4}		38 38	ns	M, S_1, S_2 = Gnd; S_0, S_3 = 4.5 V; Figs. 3-1, 3-4; Table I

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (Cont'd)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF Min	54/74LS C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to C_{n+4}		41 41	ns	M, S_0, S_3 = Gnd; S_1, S_2 = 4.5 V; Figs. 3-1, 3-4, 3-5; Table II
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to A = B		50 62	ns	M, S_0, S_3 = Gnd; S_1, S_2 = 4.5 V; R_L = 2 kΩ to 5.0 V; Figs. 3-2, 3-4, 3-5; Table II

SUM MODE TEST TABLE I **FUNCTION INPUTS:** S_0 = S_3 = 4.5 V, S_1 = S_2 = M = 0 V

SYMBOL	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

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DIFF MODE TEST TABLE II **FUNCTION INPUTS:** $S_1 = S_2 = 4.5$ V, $S_0 = S_3 = M = 0$ V

SYMBOL	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}

LOGIC MODE TEST TABLE III **FUNCTION INPUTS:** $S_1 = S_2 = M = 4.5$ V, $S_0 = S_3 = 0$ V

SYMBOL	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$