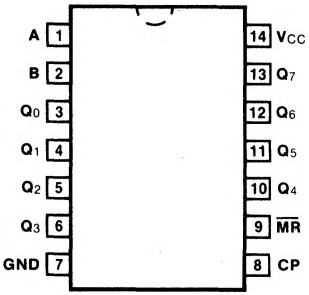
# 54/74164
# 54LS/74LS164
## SERIAL-IN PARALLEL-OUT SHIFT REGISTER

**DESCRIPTION** — The '164 is a high speed 8-bit serial-in parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds.

- **TYPICAL SHIFT FREQUENCY OF 35 MHz**
- **ASYNCHRONOUS MASTER RESET**
- **GATED SERIAL DATA INPUT**
- **FULLY SYNCHRONOUS DATA TRANSFERS**

**CONNECTION DIAGRAM**
PINOUT A



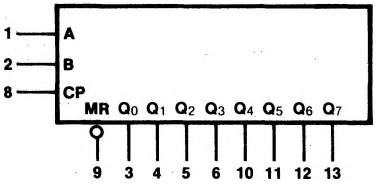

**ORDERING CODE:** See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE<br>$V_{CC}$ = +5.0 V ±5%,<br>$T_A$ = 0°C to +70°C | MILITARY GRADE<br>$V_{CC}$ = +5.0 V ±10%,<br>$T_A$ = -55°C to +125°C | PKG TYPE |
|---|---|---|---|---|
| Plastic DIP (P) | A | 74164PC, 74LS164PC | | 9A |
| Ceramic DIP (D) | A | 74164DC, 74LS164DC | 54164DM, 54LS164DM | 6A |
| Flatpak (F) | A | 74164FC, 74LS164FC | 54164FM, 54LS164FM | 3I |

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PIN NAMES | DESCRIPTION | 54/74 (U.L.) HIGH/LOW | 54/74LS (U.L.) HIGH/LOW |
|---|---|---|---|
| A, B | Data Inputs | 1.0/1.0 | 0.5/0.25 |
| CP | Clock Pulse Input (Active Rising Edge) | 1.0/1.0 | 0.5/0.25 |
| $\overline{MR}$ | Master Reset Input (Active LOW) | 1.0/1.0 | 0.5/0.25 |
| $Q_0 - Q_7$ | Outputs | 10/5.0 | 10/5.0<br>(2.5) |

**LOGIC SYMBOL**




$V_{CC}$ = Pin 14
GND = Pin 7

**FUNCTIONAL DESCRIPTION** — The '164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

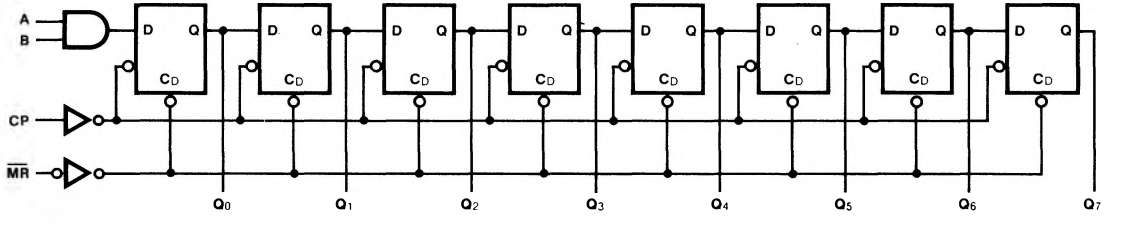
Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into $Q_0$ the logical AND of the two data inputs (A • B) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

**MODE SELECT TABLE**

| OPERATING MODE | INPUTS | | | OUTPUTS | |
|---|---|---|---|---|---|
| | $\overline{MR}$ | A | B | $Q_0$ | $Q_1 - Q_7$ |
| Reset (Clear) | L | X | X | L | L — L |
| Shift | H | l | l | L | $q_0 - q_6$ |
| | H | l | h | L | $q_0 - q_6$ |
| | H | h | l | L | $q_0 - q_6$ |
| | H | h | h | H | $q_0 - q_6$ |

L (l) = LOW Voltage Levels
H (h) = HIGH Voltage Levels
X = Immaterial
$q_n$ = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

**LOGIC DIAGRAM**



**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| SYMBOL | PARAMTER | | 54/74 Min | 54/74 Max | 54/74LS Min | 54/74LS Max | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|---|
| $I_{OS}$ | Output Short Circuit Current | XM | -10 | -27.5 | -20 | -100 | mA | $V_{CC}$ = Max |
| | | XC | -9.0 | -27.5 | -20 | -100 | | |
| $I_{CC}$ | Power Supply Current | | | 54 | | 27 | mA | A, B = Gnd, $V_{CC}$ = Max<br>CP = 2.4 V, $\overline{MR}$ = ⌐¬ |

**AC CHARACTERISTICS:** $V_{CC}$ = +5.0 V, $T_A$ = +25°C (See Section 3 for waveforms and load configurations)

| SYMBOL | PARAMETER | 54/74 $C_L$ = 15 pF, $R_L$ = 800 Ω Min | 54/74 Max | 54/74LS $C_L$ = 15 pF Min | 54/74LS Max | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Clock Frequency | 25 | | 25 | | MHz | Figs. 3-1, 3-8 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CP to $Q_n$ | | 27<br>32 | | 27<br>32 | ns | Figs. 3-1, 3-8 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CP to $Q_n$ | | 30<br>37 | | | ns | Figs. 3-1, 3-8<br>$C_L$ = 50 pF |
| $t_{PHL}$ | Propagation Delay<br>$\overline{MR}$ to $Q_n$ | | 36 | | 36 | ns | Figs. 3-1, 3-16 |
| $t_{PHL}$ | Propagation Delay<br>$\overline{MR}$ to $Q_n$ | | 42 | | | ns | Figs. 3-1, 3-16<br>$C_L$ = 50 pF |

**AC CHARACTERISTICS:** $V_{CC}$ = +5.0 V, $T_A$ = +25°C

| SYMBOL | PARAMETER | 54/74 Min | 54/74 Max | 54/74LS Min | 54/74LS Max | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|
| $t_s$ (H)<br>$t_s$ (L) | Setup Time HIGH or LOW<br>A or B to CP | 15<br>15 | | 15<br>15 | | ns | Fig. 3-6 |
| $t_h$ (H)<br>$t_h$ (L) | Hold Time HIGH or LOW<br>A or B to CP | 0<br>0 | | 5.0<br>5.0 | | ns | |
| $t_w$ (H)<br>$t_w$ (L) | CP Pulse Width HIGH or LOW | 20<br>20 | | 20<br>20 | | ns | Fig. 3-8 |
| $t_w$ (L) | $\overline{MR}$ Pulse Width LOW | 20 | | 20 | | ns | Fig. 3-16 |
| $t_{rec}$ | Recovery Time<br>$\overline{MR}$ to CP | | | 20 | | ns | Fig. 3-16 |