54/74160 • 54LS/74LS160
54/74162 • 54LS/74LS162

SYNCHRONOUS PRESETTABLE BCD DECADE COUNTERS

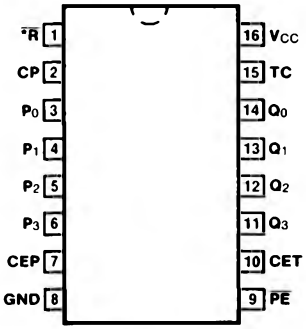
DESCRIPTION — The '160 and '162 are high speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The '160 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The '162 has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock. For the S-TTL and LP-TTL versions, please see the 9310 data sheet.

- **SYNCHRONOUS COUNTING AND LOADING**
- **HIGH SPEED SYNCHRONOUS EXPANSION**
- **TYPICAL COUNT RATE OF 35 MHz**
- **LS VERSIONS FULLY EDGE TRIGGERED**

ORDERING CODE: See Section 9

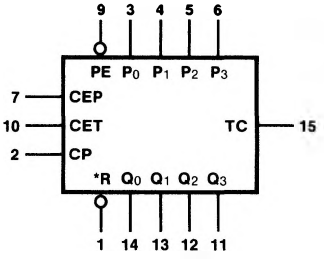
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°	PKG TYPE
Plastic DIP (P)	A	74160PC, 74LS160PC 74162PC, 74LS162PC		9B
Ceramic DIP (D)	A	74160DC, 74LS160DC 74162DC, 74LS162DC	54160DM, 54LS160DM 54162DM, 54LS162DM	7B
Flatpak (F)	A	74160FC, 74LS160FC 74162FC, 74LS162FC	54160FM, 54LS160FM 54162FM, 54LS162FM	4L

CONNECTION DIAGRAM
PINOUT A



*$\overline{MR}$ for '160
*$\overline{SR}$ for '162

LOGIC SYMBOL



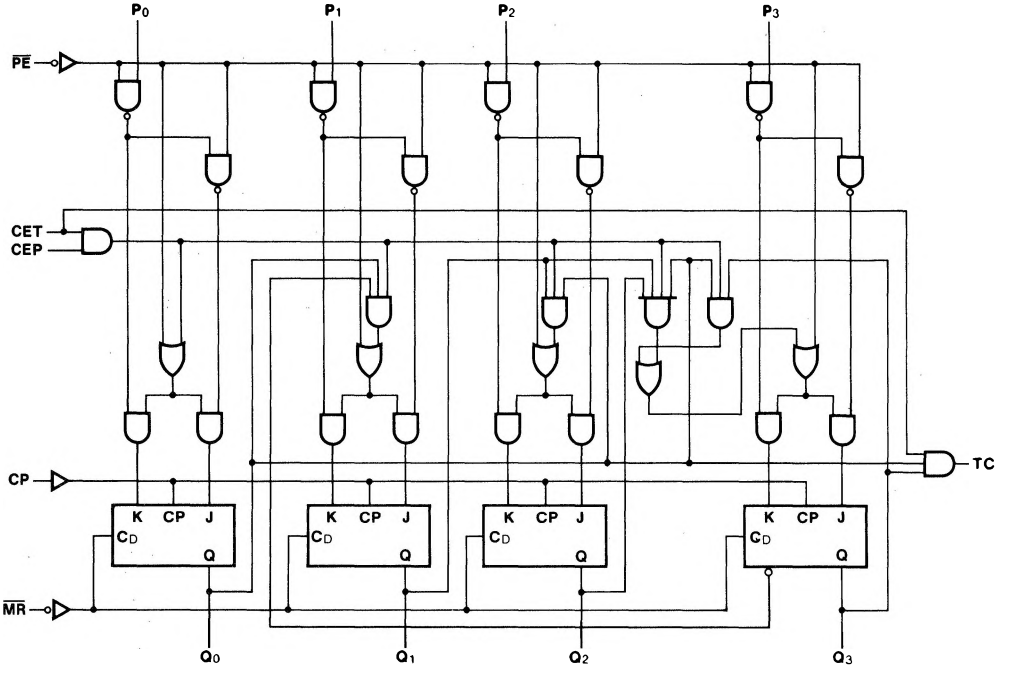
V_{CC} = Pin 16
GND = Pin 8
*$\overline{MR}$ for '160
*$\overline{SR}$ for '162

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

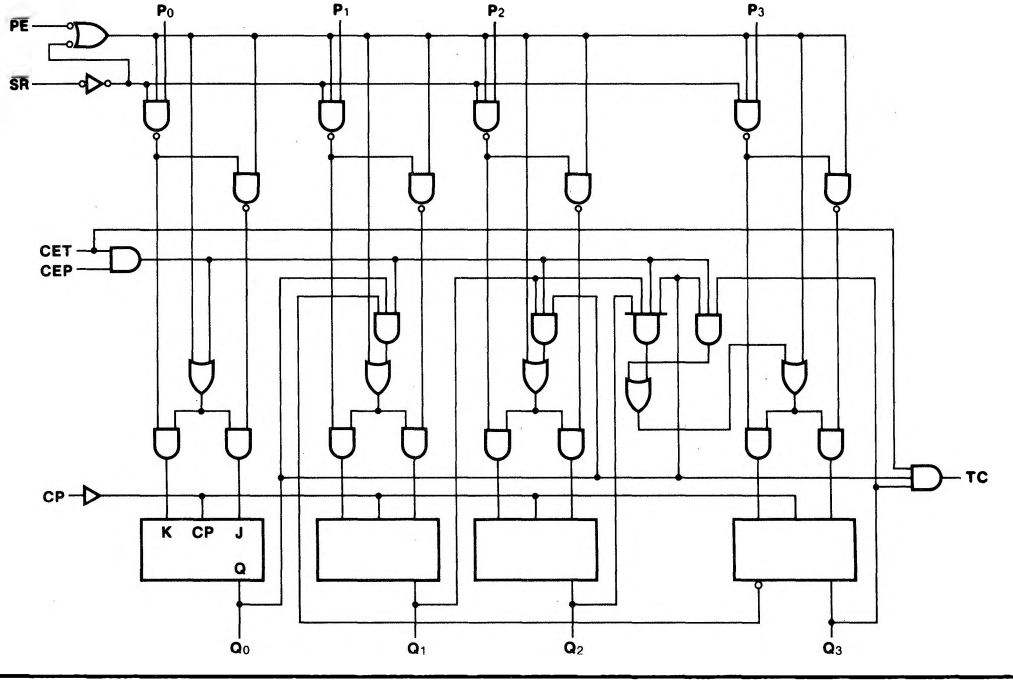
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
CEP	Count Enable Parallel Input	1.0/1.0	0.6/0.3
CET	Count Enable Trickle Input	2.0/2.0	1.0/0.5
CP	Clock Pulse Input (Active Rising Edge)	2.0/2.0	0.6/0.3
$\overline{MR}$ ('160)	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{SR}$ ('162)	Synchronous Reset Input (Active LOW)	1.0/1.0	0.5/0.25
P_0 — P_3	Parallel Data Inputs	1.0/1.0	0.5/0.25
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0	0.6/0.3
Q_0 — Q_3	Flip-flop Outputs	20/10	10/5.0 (2.5)
TC	Terminal Count Output	20/10	10/5.0 (2.5)

LOGIC DIAGRAMS

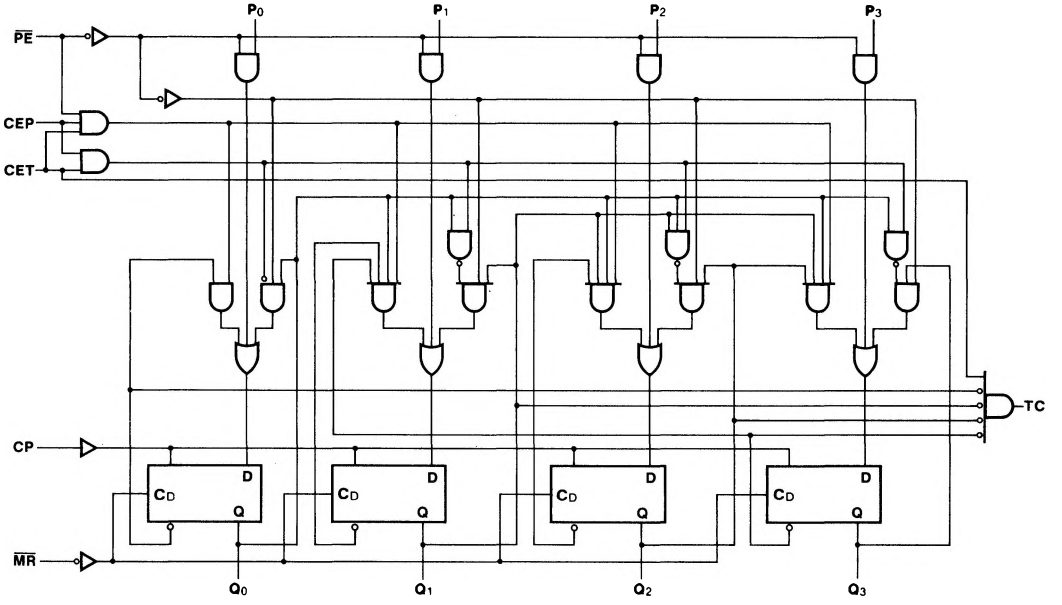
'160



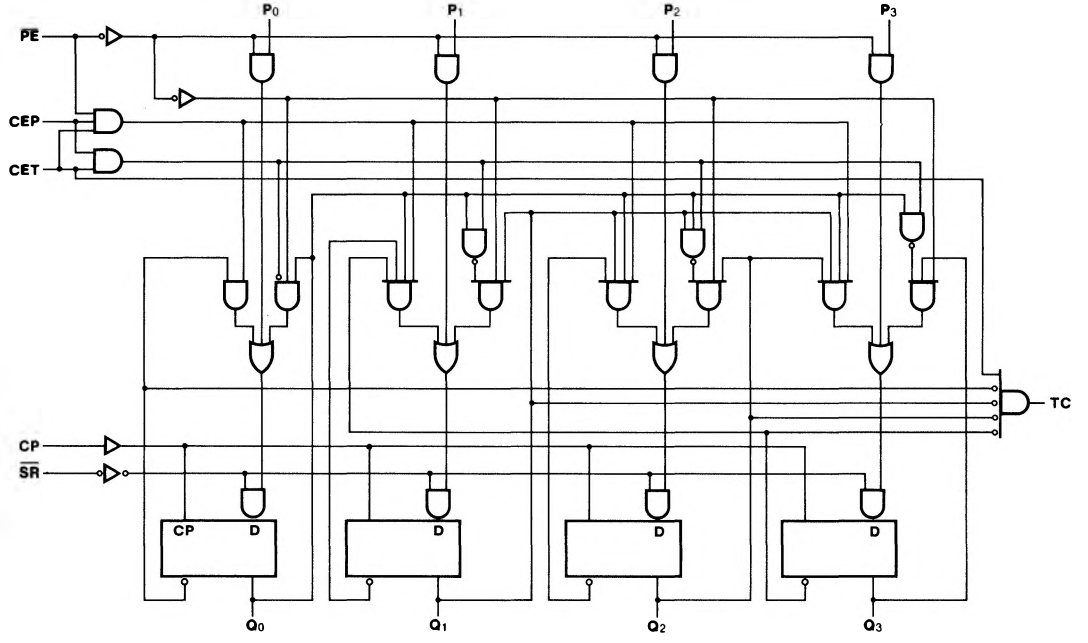
'162



LOGIC DIAGRAMS
'LS160



'LS162



FUNCTIONAL DESCRIPTION — The '160 and '162 count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The '161 and '163 count modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the '160 and '161) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('160 and '161), synchronous reset ('162 and '163), parallel load, count-up and hold. Five control inputs — Master Reset ($\overline{MR}$, '160 and '161), Synchronous Reset ($\overline{SR}$, '162 and '163), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('160, '161) or $\overline{SR}$ ('162, '163) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The TTL versions ('160 — '163, as opposed to the 'LS160 — 'LS163) contain master/slave flip-flops which are "next-state catching" because of the JK feedback. This means that when CP is LOW, information that would change the state of a flip-flop, whether from the counting logic or the parallel entry logic if either mode is momentarily enabled, enters the master and is locked in. Thus to avoid inadvertently changing the state of a master latch, and the subsequent transfer of the erroneous information to the slave when the clock rises, it is necessary to insure that neither the counting mode, the synchronous reset mode, nor the parallel entry mode is momentarily enabled while CP is LOW.

The LS-TTL versions ('LS160 — 'LS163) use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in its maximum count state (9 for the decade counters, 15 for the binary counters). To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. These two schemes are shown in the 9310 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the LS-TTL versions ('LS160, 'LS162) of the decade counters, the TC output is fully decoded and can only be HIGH in state 9. In the TTL versions ('160, '162), however, the TC output can also be HIGH in the illegal states 11, 13 and 15. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the state diagrams.

LOGIC EQUATIONS: Count Enable = CEP • CET • PE

('160, '162) $TC = Q_0 \bullet Q_3 \bullet \overline{CET}$

('LS160, 'LS162) $TC = Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3 \bullet CET$

('161, 'LS161, '163, 'LS163) $TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$

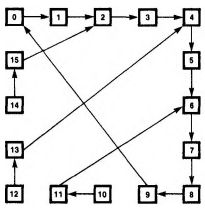
MODE SELECT TABLE

*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐‾)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

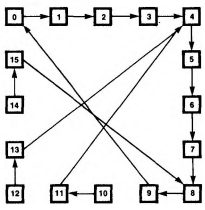
*For the '162 and '163 only.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

STATE DIAGRAMS

'160, '162



'LS160, 'LS162



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CCH}	Power Supply Current Outputs HIGH	XM		85		31	mA	V_{CC} = Max, $\overline{PE}$ = Gnd Other Inputs = 4.5 V CP = ⎍
		XC		94		31		
I_{CCL}	Power Supply Current Outputs LOW	XM		91		32	mA	V_{CC} = Max All Inputs = Gnd CP = ⎍
		XC		101		32		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
f_{max}	Maximum Count Frequency	25		25		MHz	Figs. 3-1, 3-8
t_{PLH}	Propagation Delay CP to TC		35		25	ns	Figs. 3-1, 3-8
t_{PHL}			35		21		
t_{PLH}	Propagtion Delay CP to Q_n		20		24	ns	Figs. 3-1, 3-8 $\overline{PE}$ = 4.5 V
t_{PHL}			23		27		
t_{PLH}	Propagtion Delay CP to Q_n		25		24	ns	Figs. 3-1, 3-8 $\overline{PE}$ = Gnd
t_{PHL}			29		27		
t_{PLH}	Propagation Delay CET to TC		16		14	ns	Figs. 3-1, 3-5
t_{PHL}			16		23		
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('160 and '161)		38		28	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW P_n to CP	20 20		20 20		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time, HIGH or LOW P_n to CP	0 0		5.0 5.0		ns	
t_s (H) t_s (L)	Setup Time, HIGH or LOW $\overline{PE}$ to CP	25 25		25 25		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{PE}$ to CP	0 0		0 0		ns	
t_s (H) t_s (L)	Setup Time, HIGH or LOW CEP, CET or $\overline{SR}$ to CP	20 20		25 25		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time, HIGH or LOW CEP, CET or $\overline{SR}$ to CP	0 0		0 0		ns	
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	15 25		15 25		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW ('160 and '161)	20		15		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP ('160 and '161)			20		ns	Fig. 3-16