FAIRCHILD SEMICONDUCTOR™

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74LCX374
Low Voltage Octal D Flip-Flop with 5V Tolerant Inputs and Outputs

General Description

The LCX374 consists of eight D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The LCX374 is designed for low-voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

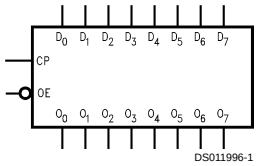
- 5V tolerant inputs and outputs
- 8.5 ns t_{PD} max, 10 µA I_{CCQ} max
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented noise/EMI reduction circuitry
- Functionally compatible with the 74 series 374
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human Body Model > 2000V
  Machine Model > 200V

Ordering Code:

Order Number	Package Number	Package Description
74LCX374WM	M20B	20-Lead (0.300" Wide) Molded Small Outline Package SOIC JEDEC
74LCX374SJ	M20D	20-Lead Small Outline Package SOIC EIAJ
74LCX374MSA	MSA20	20-Lead Molded Shrink Small Outline Package SSOP Type II
74LCX374MTC	MTC20	20-Lead Thin Shrink Small Outline Package TSSOP JEDEC

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



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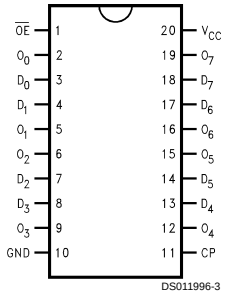
Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	Output Enable Input
O_0–O_7	3-STATE Outputs

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



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Functional Description

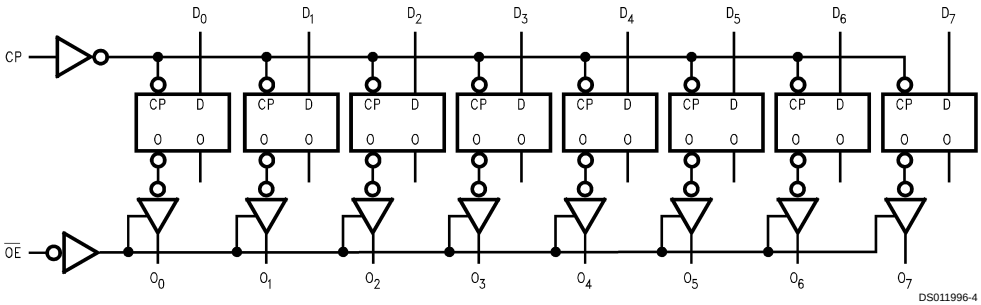
The LCX374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	L	L	O_0
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
O_0 = Previous O_0 before HIGH to LOW of CP

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		˚C

Recommended Operating Conditions (Note 3)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V		±24	mA
		V_{CC} = 2.7V		±12	
T_A	Free-Air Operating Temperature		−40	85	˚C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Note 3: Unused inputs or I/Os must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40^\circ C$ to $+85^\circ C$		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100$ µA	2.7–3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -12$ mA	2.7	2.2		V
		$I_{OH} = -18$ mA	3.0	2.4		V
		$I_{OH} = -24$ mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100$ µA	2.7–3.6		0.2	V
		$I_{OL} = 12$ mA	2.7		0.4	V
		$I_{OL} = 16$ mA	3.0		0.4	V
		$I_{OL} = 24$ mA	3.0		0.55	V
I_I	Input Leakage Current	$0 \le V_I \le 5.5V$	2.7–3.6		±5.0	µA
I_{OZ}	3-STATE Output Leakage	$0 \le V_O \le 5.5V$ $V_I = V_{IH}$ or V_{IL}	2.7–3.6		±5.0	µA
I_{OFF}	Power-Off Leakage Current	V_I or $V_O = 5.5V$	0		10	µA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7–3.6		10	µA
		$3.6V \le V_I$, $V_O \le 5.5V$	2.7–3.6		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7–3.6		500	µA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40^\circ C$ to $+85^\circ C$, $C_L = 50pF$, $R_L = 500\ \Omega$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	150				MHz
t_{PHL}	Propagation Delay	1.5	8.5	1.5	9.5	ns
t_{PLH}	CP to O_n	1.5	8.5	1.5	9.5	
t_{PZL}	Output Enable Time	1.5	8.5	1.5	9.5	ns
t_{PZH}		1.5	8.5	1.5	9.5	
t_{PLZ}	Output Disable Time	1.5	7.5	1.5	8.5	ns
t_{PHZ}		1.5	7.5	1.5	8.5	
t_S	Setup Time	2.5		2.5		ns
t_H	Hold Time	1.5		1.5		ns
t_W	Pulse Width	3.3		3.3		ns
t_{OSHL}	Output to Output Skew (Note 4)		1.0			ns
t_{OSLH}			1.0			

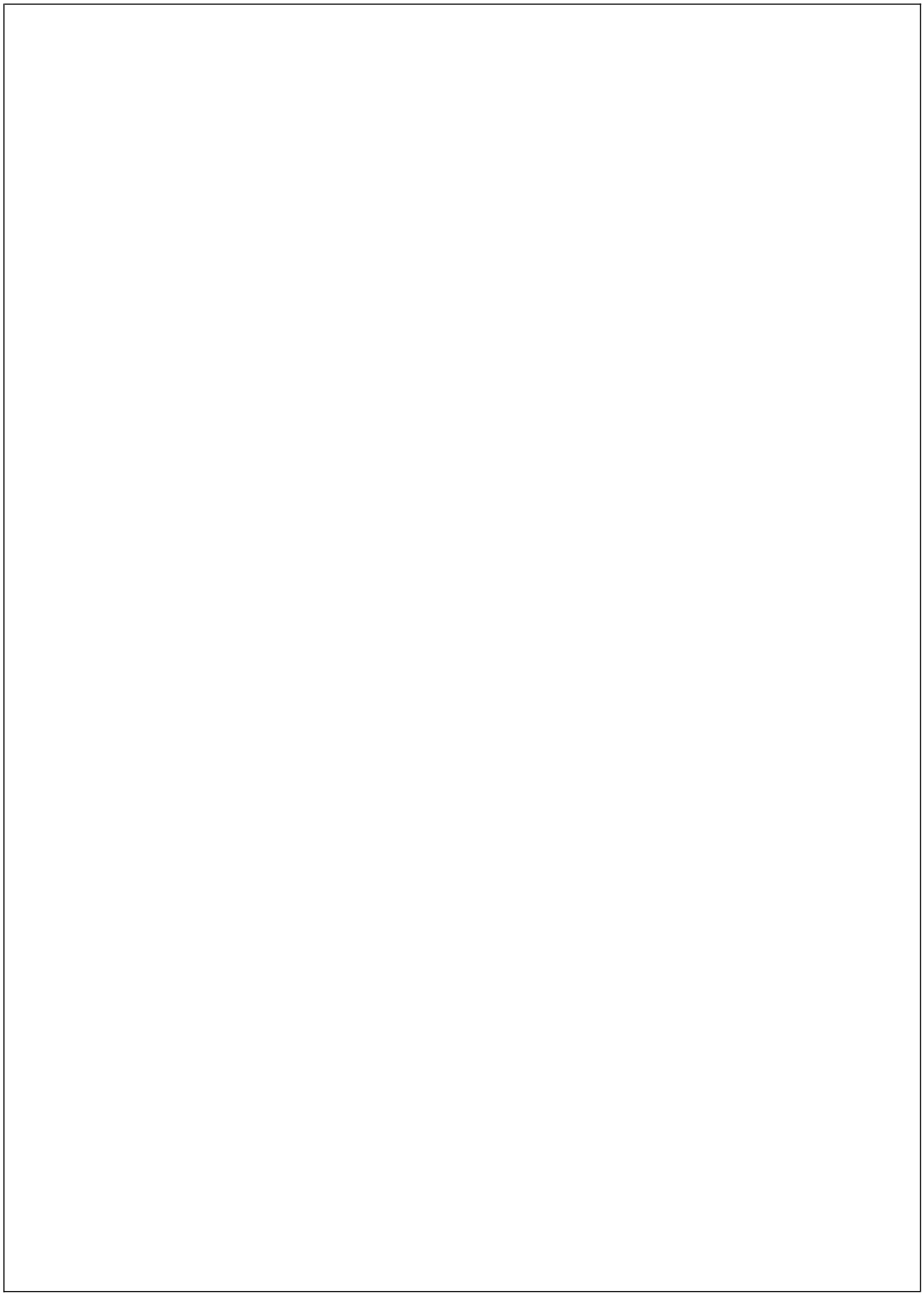
Note 4: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

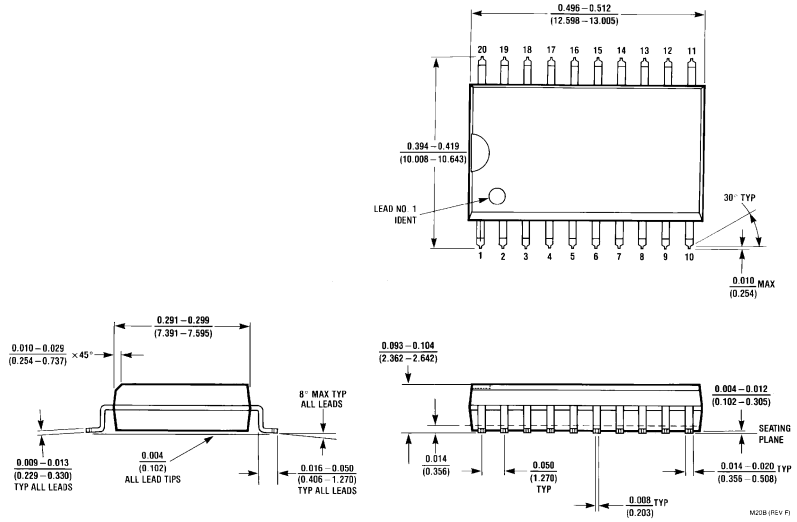
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25^\circ C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	−0.8	V

Capacitance

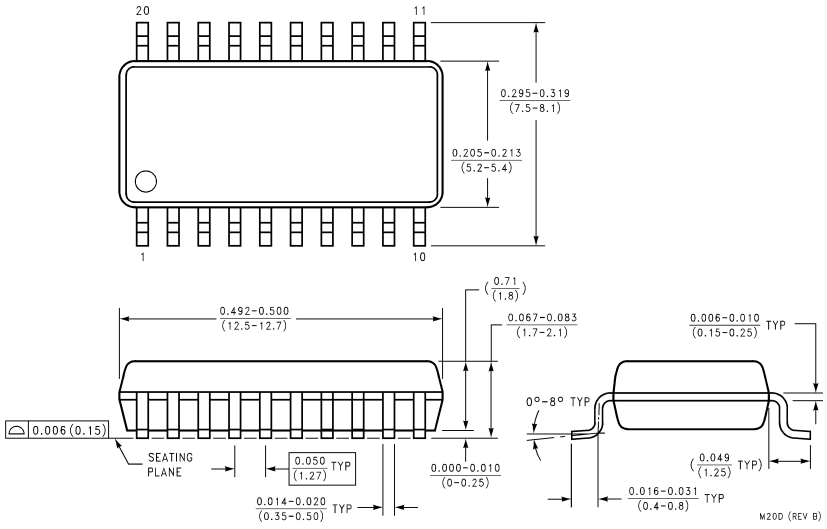
Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10 MHz	25	pF



Physical Dimensions inches (millimeters) unless otherwise noted

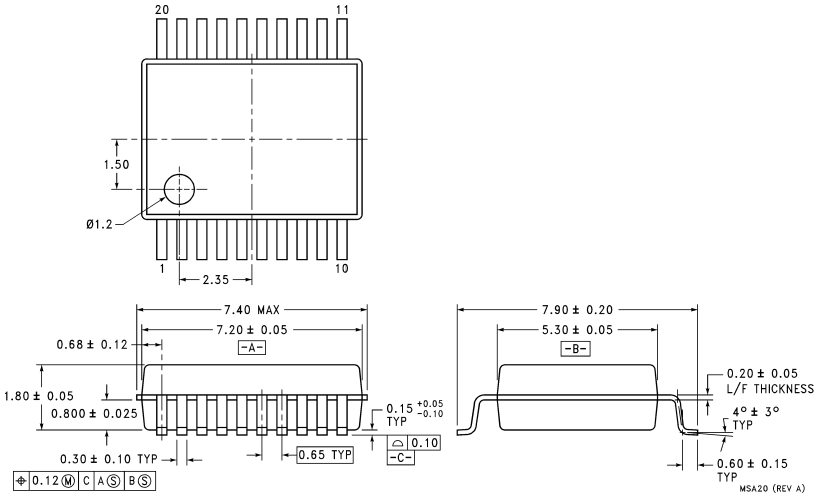


20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC
Package Number M20B



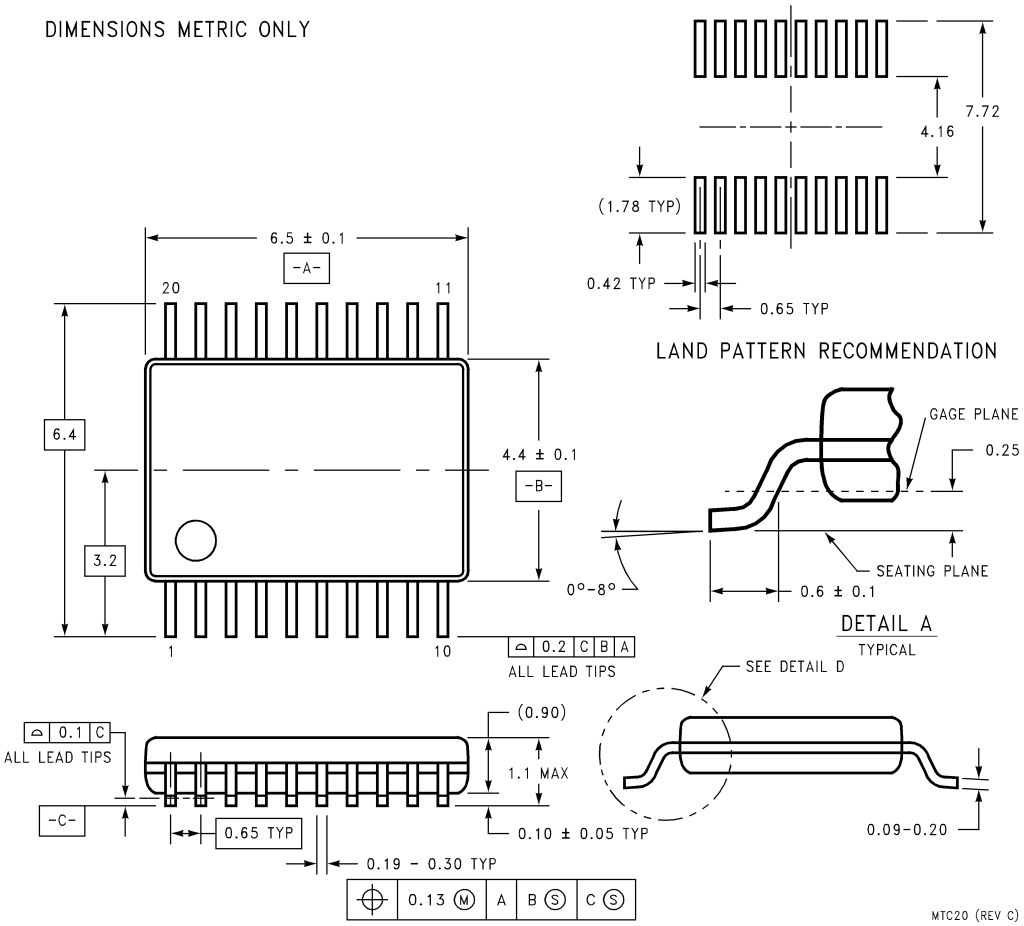
20-Lead Small Outline Package, EIAJ (SJ)
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Molded Shrink Small Outline Package, EIAJ, Type II
Package Number MSA20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Thin Shrink Small Outline Package, JEDEC
Package Number MTC20

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Corporation
Americas
Customer Response Center
Tel: 1-888-522-5372

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

www.fairchildsemi.com