DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT244

Octal buffer/line driver; 3-state

Product specification

File under Integrated Circuits, IC06

December 1990

**Philips
Semiconductors**

PHILIPS

PHILIPS

Octal buffer/line driver; 3-state

74HC/HCT244

FEATURES

- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT244 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT244 are octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The "244" is identical to the "240" but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 5 V	9	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	35	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC   the condition is V_I = GND to V_{CC}

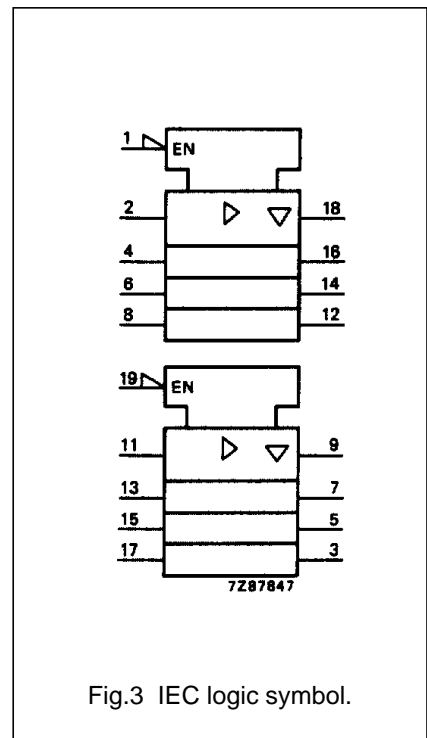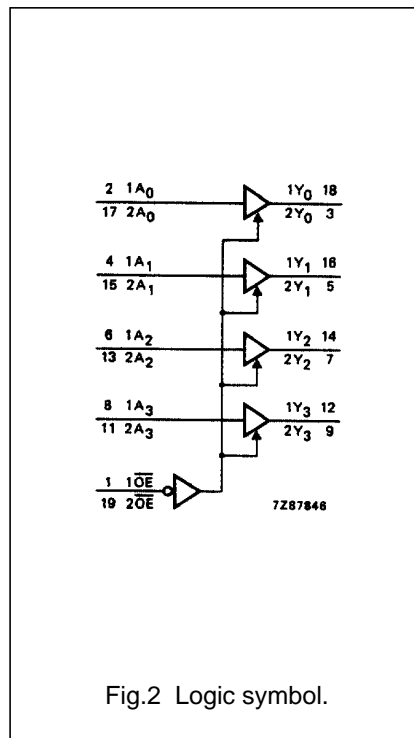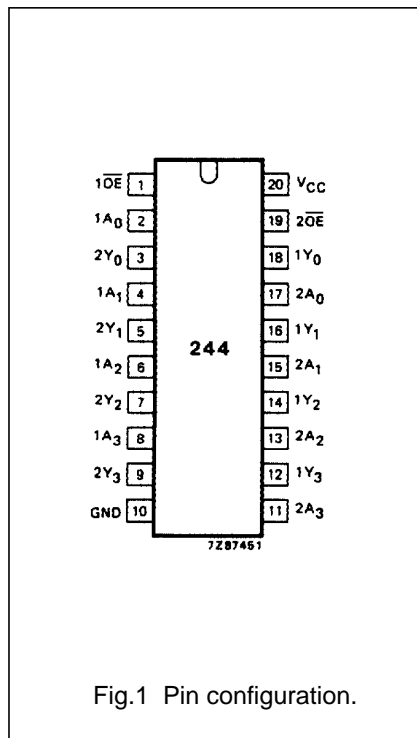   For HCT the condition is V_I = GND to $V_{CC} - 1.5$ V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

Octal buffer/line driver; 3-state

74HC/HCT244

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	$2\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

Fig.1 Pin configuration.

Fig.2 Logic symbol.

Fig.3 IEC logic symbol.

Octal buffer/line driver; 3-state

74HC/HCT244

Fig.4 Functional diagram.
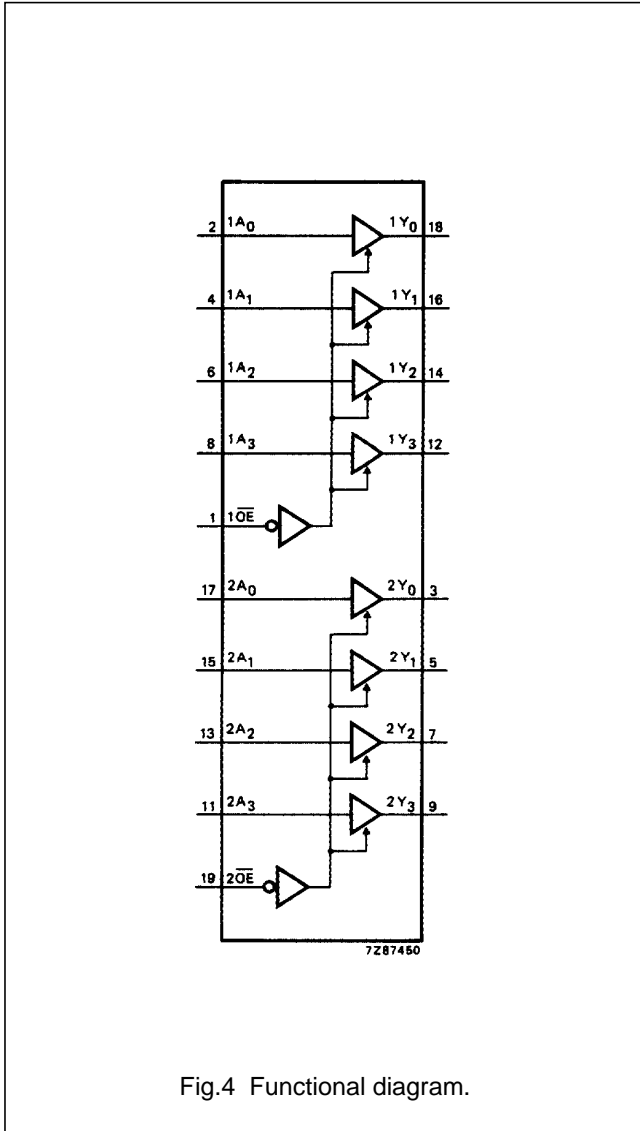
FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	L
L	H	H
H	X	Z

Note

1. H = HIGH voltage level
    L = LOW voltage level
    X = don't care
    Z = high impedance OFF-state