

# 54H/74H101

## JK EDGE-TRIGGERED FLIP-FLOP (with AND-OR Inputs)

**DESCRIPTION** — The '101 is a high speed JK negative edge-triggered flip-flop. The AND-OR gate inputs are inhibited while the clock input is LOW. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic state of J and K inputs may be allowed to change when the clock pulse is in a HIGH state and the bistable will perform according to the Truth Table as long as minimum setup times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

### TRUTH TABLE

INPUTS		OUTPUT
@ $t_n$	@ $t_n + 1$	Q
J	K	Q
L	L	$Q_n$
L	H	L
H	L	H
H	H	$\bar{Q}_n$

Asynchronous Input:

LOW input to  $\bar{S}_D$  sets Q to HIGH level  
Set is independent of clock

$J = (J_{1A} \cdot J_{1B}) + (J_{2A} \cdot J_{2B})$   
 $K = (K_{1A} \cdot K_{1B}) + (K_{2A} \cdot K_{2B})$   
 $t_n$  = Bit time before clock pulse.  
 $t_{n+1}$  = Bit time after clock pulse.  
 H = HIGH Voltage Level  
 L = LOW Voltage Level

**ORDERING CODE:** See Section 9

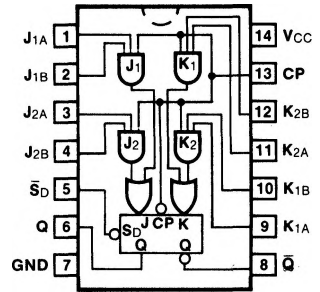
PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 V \pm 5\%$ , $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = +5.0 V \pm 10\%$ , $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP (P)	A	74H101PC		9A
Ceramic DIP (D)	A	74H101DC	54H101DM	6A
Flatpak (F)	B	74H101FC	54H101FM	3I

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

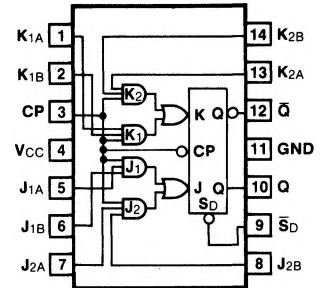
PIN NAMES	DESCRIPTION	54/74H (U.L.) HIGH/LOW
J <sub>1A</sub> , J <sub>1B</sub> , J <sub>2A</sub> , J <sub>2B</sub> K <sub>1A</sub> , K <sub>1B</sub> , K <sub>2A</sub> , K <sub>2B</sub>	Data Inputs	1.25/1.25
$\bar{C}P$	Clock Pulse Input (Active Falling Edge)	0*/3.0
$\bar{S}_D$	Direct Set Input (Active LOW)	2.5/1.25
Q, $\bar{Q}$	Outputs	12.5/12.5

\* $\bar{C}P$  Sourcing Current, see DC Characteristics Table

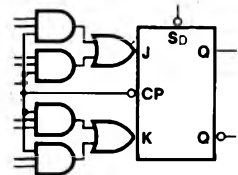
### CONNECTION DIAGRAMS PINOUT A



### PINOUT B

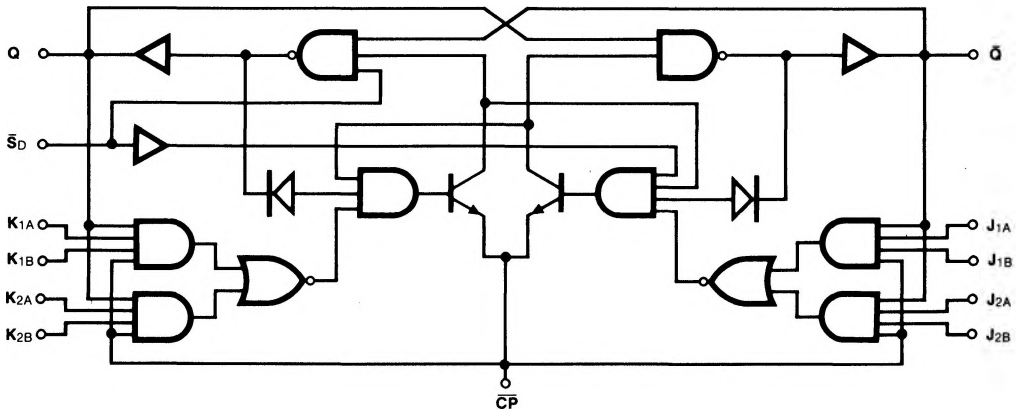


### LOGIC SYMBOL



$V_{CC}$  = Pin 14  
GND = Pin 7

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74H		UNITS	CONDITIONS
		Min	Max		
$I_{IH}$	Input HIGH Current at $\overline{CP}$	0	-1.0	mA	$V_{CC} = \text{Max}, V_{CP} = 2.4 \text{ V}$
$I_{CC}$	Power Supply Current		38	mA	$V_{CC} = \text{Max}, V_{CP} = 0 \text{ V}$

AC CHARACTERISTICS:  $V_{CC} = +5.0 \text{ V}, T_A = +25^\circ \text{C}$  (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74H		UNITS	CONDITIONS
		$C_L = 25 \text{ pF}$ $R_L = 280 \Omega$			
		Min	Max		
$f_{max}$	Maximum Clock Frequency	40		MHz	Figs. 3-1, 3-9
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{CP}$ to Q or $\overline{Q}$		15 20	ns	Figs. 3-1, 3-9
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_D$ to Q or $\overline{Q}$		12 20	ns	$V_{CP} \geq 2.0 \text{ V}$ Figs. 3-1, 3-10
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{S_D}$ to Q or $\overline{Q}$		12 35	ns	$V_{CP} \leq 0.8 \text{ V}$ Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS:  $V_{CC} = +5.0 \text{ V}, T_A = +25^\circ \text{C}$

SYMBOL	PARAMETER	54/74H		UNITS	CONDITIONS
		Min	Max		
$t_s$ (H) $t_s$ (L)	Setup Time $J_n$ or $K_n$ to $\overline{CP}$	10 13		ns	Fig. 3-7
$t_h$ (H) $t_h$ (L)	Hold Time $J_n$ or $K_n$ to $\overline{CP}$	0 0		ns	
$t_w$ (H) $t_w$ (L)	$\overline{CP}$ Pulse Width	10 15		ns	Fig. 3-9
$t_w$ (L)	$\overline{S_D}$ Pulse Width LOW	16		ns	Fig. 3-10