National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT841A•54FCT/74FCT841B
10-Bit Transparent Latch with TRI-STATE® Outputs

General Description

The bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'FCT841A/B is a 10-bit transparent latch, a 10-bit version of the FCT373A.

FACT™ FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

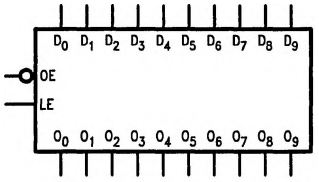
FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

Features

- NSC 54FCT/74FCT841A/B is pin and functionally equivalent to IDT 54FCT/74FCT841A/B
- High Speed parallel latches
- Buffered common latch enable, clear and preset input
- Input clamp diodes to limit bus reflections
- TIL/CMOS input and output level compatible
- I_{OL} = 48 mA (com), 32 mA (mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

Logic Symbols



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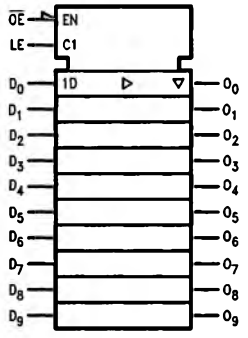

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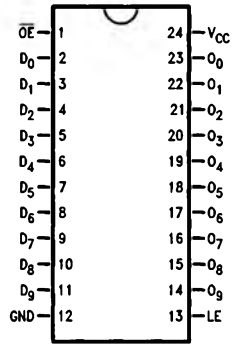
Pin Names	Description
D_0–D_9	Data Inputs
O_0–O_9	TRI-STATE Outputs
$\overline{OE}$	Output Enable
LE	Latch Enable

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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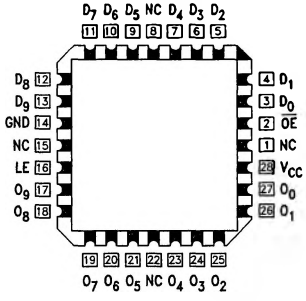
Pin Assignment for LCC



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