National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT825A • 54FCT/74FCT825B
8-Bit D Flip-Flop

General Description

The 'FCT825A/B is an 8-bit buffered register. They have Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included are multiple enables that allow multiuse control of the interface.

FACT™ FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

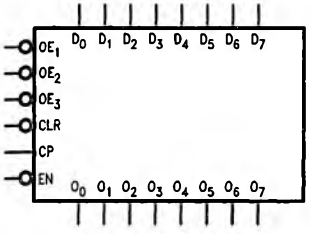
FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

Features

- NSC 54FCT/74FCT825A/B is pin and functionally equivalent to IDT 54FCT/74FCT825A/B
- High-speed parallel registers with positive edge-triggered D-type flip flops
- Buffered common clock enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

Logic Symbols



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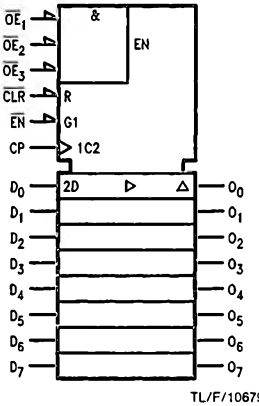
IEEE/IEC



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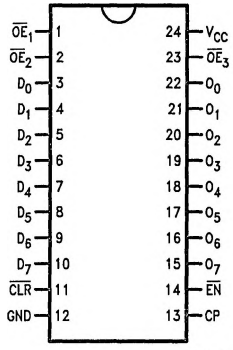
Pin Names	Description
D_0–D_7	Data Inputs
O_0–O_7	Data Outputs
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$	Output Enables
$\overline{EN}$	Clock Enable
$\overline{CLR}$	Clear
CP	Clock Input

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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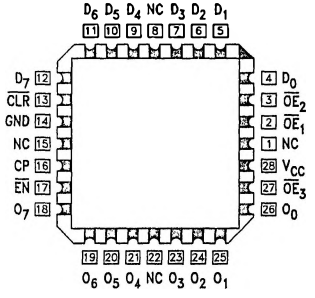
Pin Assignment for LCC



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