National Semiconductor

54F/74F968
1 Mbit Dynamic RAM Controller

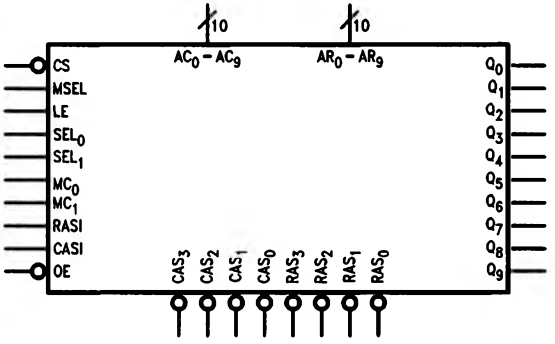
General Description

The 'F968 is a high performance memory controller, replacing many SSI and MSI devices by grouping several unique functions. It provides two 10-bit address latches and two 10-bit counters for row and column address generation during refresh. A 2-bit bank select latch for row and column address generation during refresh and a 2-bit bank select latch for the two high order address bits are provided to select one of the four RAS and CAS outputs.

Features

- Provides control for 16k, 64k, 256k or 1 Mbit DRAM systems
- Outputs directly drive up to 88 DRAMs
- Chip select for easy expansion
- Provides memory refresh with error correction mode
- 52-pin plastic leaded chip carrier

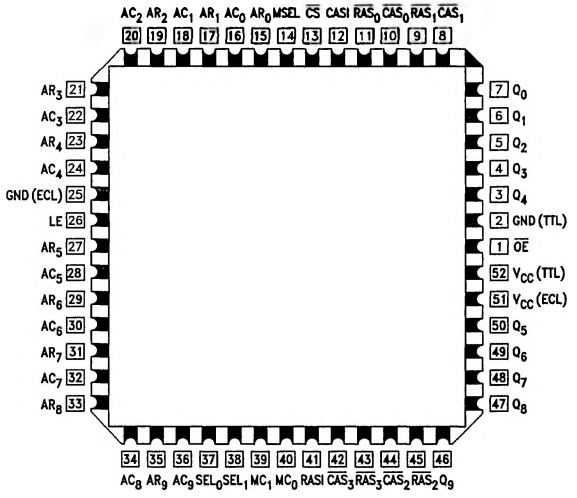
Logic Symbol



TL/F/9604–1

Connection Diagram

Pin Assignment for PCC



TL/F/9604–3

Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
AC_0–AC_9	Column Address Inputs	1.0/1.0	20 μA/−0.6 mA
AR_0–AR_9	Row Address Inputs	1.0/1.0	20 μA/−0.6 mA
MC_0, MC_1	Mode Control Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{CS}$	Chip Select Input	1.0/1.0	20 μA/−0.6 mA
MSEL	Multiplexer Select Input	1.0/1.0	20 μA/−0.6 mA
LE	Latch Enable Input	1.0/1.0	20 μA/−0.6 mA
SEL_0, SEL_1	Bank Select Inputs	1.0/1.0	20 μA/−0.6 mA
RASI	Row Address Strobe In	1.0/1.0	20 μA/−0.6 mA
CASI	Column Address Strobe In	1.0/1.0	20 μA/−0.6 mA
$\overline{OE}$	Output Enable	1.0/1.0	20 μA/−0.6 mA
$\overline{RAS}_0$–$\overline{RAS}_3$	Row Address Strobe Outputs	150/1.667	−3 mA/1.0 mA
$\overline{CAS}_0$–$\overline{CAS}_3$	Column Address Strobe Outputs	150/1.667	−3 mA/1.0 mA
Q_0–Q_9	Address Outputs	150/1.667	−3 mA/1.0 mA

Pin Description

Name	I/O	Description
AR_0–AR_9 AC_0–AC_9	I	**Address Inputs.** AR_0–AR_9 are latched in as the 10-bit Row Address for the RAM. These inputs drive Q_0–Q_9 when the 'F968 is in the Read/Write mode and MSEL is LOW. AC_0–AC_9 are latched in as the Column Address, and will drive Q_0–Q_9 when MSEL is HIGH and the 'F968 is in the Read/Write mode. The addresses are latched with the Latch Enable (LE) signal.
SEL_0–SEL_1	I	**Bank Select.** These two inputs are normally the two higher order address bits, and are used in the Read/Write mode to select which bank of memory will be receiving the $\overline{RAS}_n$ and $\overline{CAS}_n$ signals after RASI and CASI go HIGH.
LE	I	**Latch Enable.** This active-HIGH input causes the Row, Column and Bank Select latches to become transparent, allowing the latches to accept new input data. A LOW input on LE latches the input data, assuming it meets the setup and hold time requirements.
MSEL	I	**Multiplexer Select.** This input determines whether the Row or Column Address will be sent to the memory address inputs. When MSEL is HIGH the Column Address is selected, while the Row Address is selected when MSEL is LOW. The address may come from either the address latch or refresh address counter depending on MC_0, MC_1.
$\overline{CS}$	I	**Chip Select.** This active-LOW input is used to enable the 'F968. When $\overline{CS}$ is active, the 'F968 operates normally in all four modes. When $\overline{CS}$ goes HIGH, the device will not enter the Read/Write mode. This allows other devices to access the same memory that the 'F968 is controlling (e.g., DMA controller).
$\overline{OE}$	I	**Output Enable.** This active-LOW input enables/disables the output signals. When $\overline{OE}$ is HIGH, the outputs of the 'F968 enter the high impedance state. The $\overline{OE}$ signal allows more than one 'F968 to control the same memory, thus providing an easy method to expand the memory size.
MC_0, MC_1	I	**Mode Control.** These inputs are used to specify which of the four operating modes the 'F968 should be using. The description of the four operating modes is given in the Mode Control Function Table.
Q_0–Q_9	O	**Address Outputs.** These address outputs will feed the DRAM address inputs and provide drive for memory systems up to 500 pF in capacitance.
RASI	I	**Row Address Strobe Input.** During normal memory cycles, the decoded $\overline{RAS}_n$ output ($\overline{RAS}_0$, $\overline{RAS}_1$, $\overline{RAS}_2$ or $\overline{RAS}_3$) is forced LOW after receipt of RASI. In either refresh mode, all four $\overline{RAS}_n$ outputs will go LOW following RASI going HIGH.
$\overline{RAS}_0$–$\overline{RAS}_3$	O	**Row Address Strobe.** Each one of the Row Address Strobe outputs provides a $\overline{RAS}_n$ signal to one of the four banks of dynamic memory. Each will go LOW only when selected by SEL_0 and SEL_1 and only after RASI goes HIGH. All four go LOW in response to RASI in either of the Refresh modes.
CASI	I	**Column Address Strobe Input.** This input going active will cause the selected $\overline{CAS}_n$ output to be forced LOW.
$\overline{CAS}_0$–$\overline{CAS}_3$	O	**Column Address Strobe.** During normal Read/Write cycles the two select bits (SEL_0, SEL_1) determine which $\overline{CAS}_n$ output will go active following CASI going HIGH. When memory error correction is performed, only the $\overline{CAS}_n$ signal selected by $CNTR_0$ and $CNTR_1$ will be active. For non-error correction cycles, all four $\overline{CAS}_n$ outputs remain HIGH.

Functional Description

The 74F968 is a 1 Mbit DRAM controller which is functionally equivalent to AMD's Am29368. The 74F968 provides row-/column address multiplexing, refresh address generation and bank selection for up to four banks of RAMs.

Twenty-two (22) address bits (AR_0–AR_9, AC_0–AC_9 and bank select addresses SEL_0 and SEL_1) are presented to the controller. These addresses are latched by a 22-bit latch. A 22-bit counter generates the refresh address.

A 10-bit multiplexer selects the output address between the input row address, column address, refresh counter row address, column address, or zero (clear). Four RAS and four CAS outputs select the appropriate bank of RAMs and strobe in the row and column addresses.

It should be noted that the counters are cleared (MC_0, MC_1 = 1, 1) on the next RASI transition, but the Q outputs are asynchronously cleared through the multiplexer.

Mode Control Function Table

MC_1	MC_0	Operating Mode
L	L	**Refresh without Error Correction—** Refresh cycles are performed with only the Row Counter being used to generate addresses. In this mode, all four $\overline{RAS}_n$ outputs are active while the four $\overline{CAS}_n$ signals are kept HIGH.
L	H	**Refresh with Error Correction/Initialize—** During this mode, refresh cycles are done with both the Row and Column counters generating the addresses. MSEL is used to select between the Row and Column counter. All four $\overline{RAS}_n$ outputs go active in response to RASI, while only one $\overline{CAS}_n$ output goes LOW in response to CASI. The Bank Counter keeps track of which $\overline{CAS}_n$ output will go active. This mode of operation is possible when supported by an error detection/correction circuit such as the 'F632.
H	L	**Read/Write—** This mode is used to perform Read/Write cycles. Both the Row and Column addresses are latched and multiplexed to the address output lines using MSEL; SEL_0 and SEL_1 are decoded to determine which $\overline{RAS}_n$ and $\overline{CAS}_n$ will be active.
H	H	**Clear Refresh Counter—** This mode will clear the three refresh counters (Row, Column and Bank) on the HIGH-to-LOW transition of RASI, putting them at the start of the refresh sequence. In this mode, all four $\overline{RAS}_n$ outputs are driven LOW upon receipt of RASI so that DRAM wake-up cycles are performed. This mode also asynchronously clears the Q_n outputs.

H = HIGH Voltage Level
L = LOW Voltage Level

Address Output Function Table

$\overline{CS}$	MC_1	MC_0	MSEL	Mode	MUX Output
L	L	L	X	Refresh without Error Correction	Row Counter Address
	L	H	H	Refresh with Error Correction	Column Counter Address
			L		Row Counter Address
	H	L	H	Read/Write	Column Address Latch
			L		Row Address Latch
	H	H	X	Clear Refresh Counter	Zero
H	L	L	X	Refresh without Error Correction	Row Counter Address
	L	H	H	Refresh with Error Correction	Column Counter Address
			L		Row Counter Address
	H	L	X	Read/Write	Zero
	H	H	X	Clear Refresh Counter	Zero

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

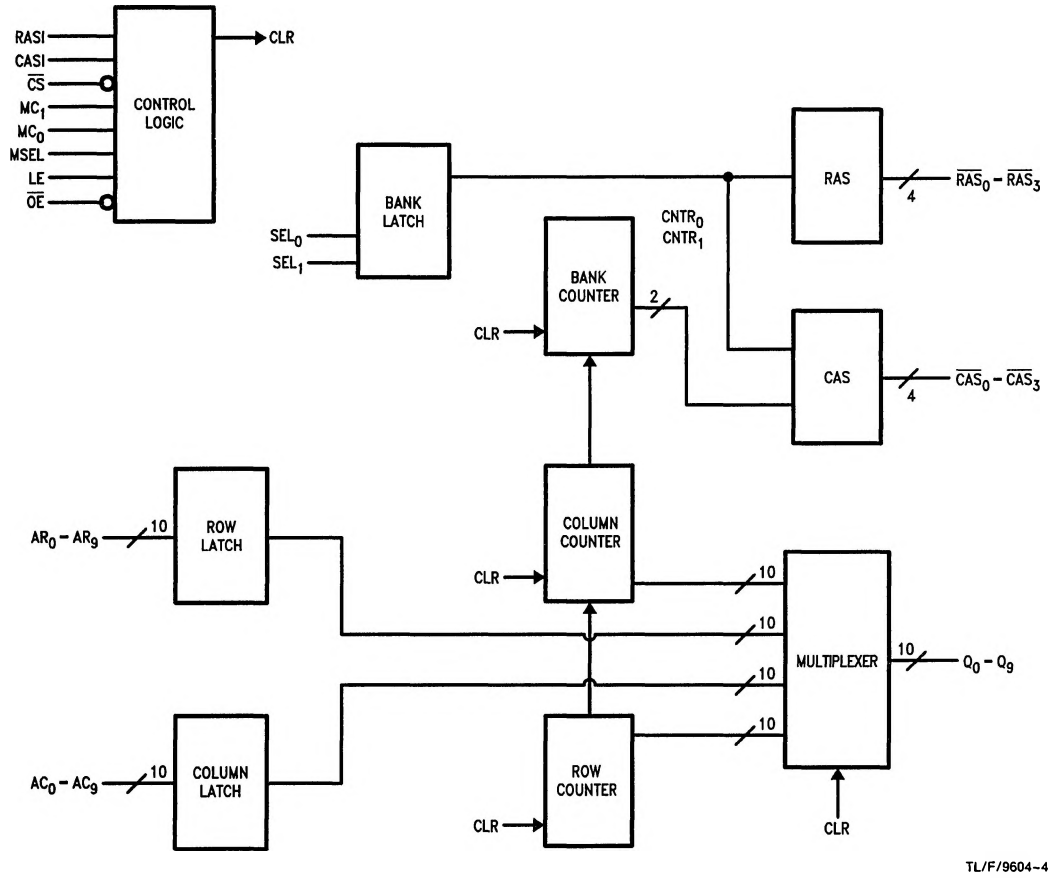
$\overline{RAS}$ Output Function Table

RASI	$\overline{CS}$	MC_1	MC_0	SEL_1	SEL_0	Mode	$\overline{RAS}_0$	$\overline{RAS}_1$	$\overline{RAS}_2$	$\overline{RAS}_3$
L	X	X	X	X	X	Non-Refresh	H	H	H	H
H	L	L	L	X	X	Refresh without Error Correction	L	L	L	L
		L	H	X	X	Refresh with Error Correction	L	L	L	L
		H	L	L	L	Read/Write	L	H	H	H
				L	H		H	L	H	H
				H	L		H	H	L	H
				H	H		H	H	H	L
		H	H	X	X	Clear Refresh Counter	L	L	L	L
	H	L	L	X	X	Refresh without Error Correction	L	L	L	L
		L	H			Refresh with Error Correction	L	L	L	L
		H	L			Read/Write	H	H	H	H
		H	H			Clear Refresh Counter	L	L	L	L

$\overline{CAS}$ Output Function Table

Inputs				Internal Counter		Inputs		Outputs			
CASI	$\overline{CS}$	MC_1	MC_0	$CNTR_1$	$CNTR_0$	SEL_1	SEL_0	$\overline{CAS}_0$	$\overline{CAS}_1$	$\overline{CAS}_2$	$\overline{CAS}_3$
H	L	L	L	X	X	X	X	H	H	H	H
		L	H	L	L	X	X	L	H	H	H
				L	H			H	L	H	H
				H	L			H	H	L	H
				H	H			H	H	H	L
		H	L	X	X	L	L	L	H	H	H
						L	H	H	L	H	H
						H	L	H	H	L	H
						H	H	H	H	H	L
		H	H	X	X	X	X	H	H	H	H
	H	L	L	X	X	X	X	H	H	H	H
		L	H	L	L	X	X	L	H	H	H
				L	H			H	L	H	H
				H	L			H	H	L	H
				H	H			H	H	H	L
		H	L	X	X	X	X	H	H	H	H
		H	H								
L	X	X	X	X	X	X	X	H	H	H	H

Block Diagram



Memory Cycle Timing

The relationship between the 'F968 specifications and system timing requirements is shown in *Figures 1–6*. T1, T2 and T3 represent the minimum timing requirements at the 'F968 inputs to guarantee that the RAM timing requirements are met and that maximum system performance is achieved.

The minimum requirement for T1, T2 and T3 are as follows:

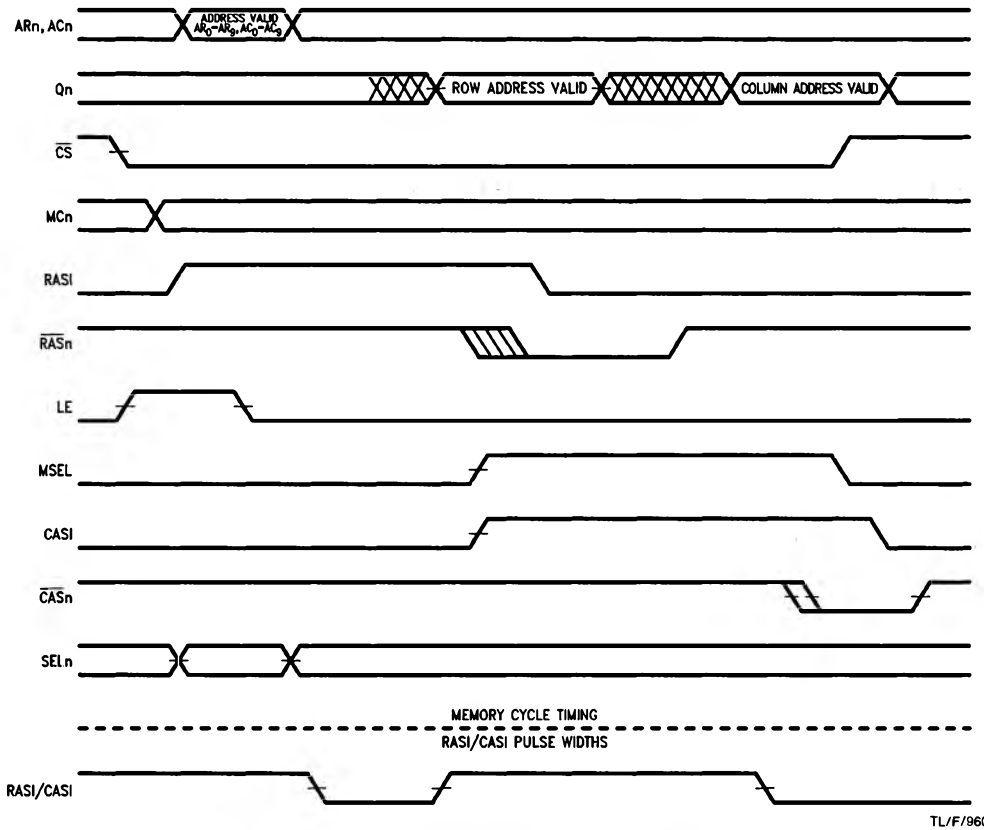
T1 Min = $t_{ASR} + t_{skew}$

T2 Min = $t_{RAH} + t_{skew}$

T3 Min = T2 + $t_{skew} + t_{ASC}$.

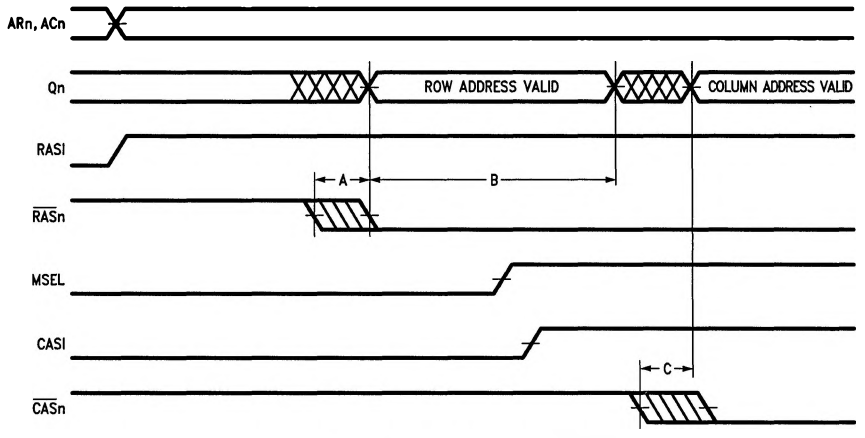
See RAM data sheet for applicable values for t_{RAH}, t_{ASC} and t_{ASR}.

Memory Cycle Timing (Continued)



TL/F/9604–5

FIGURE 1. Dynamic Memory Controller Timing

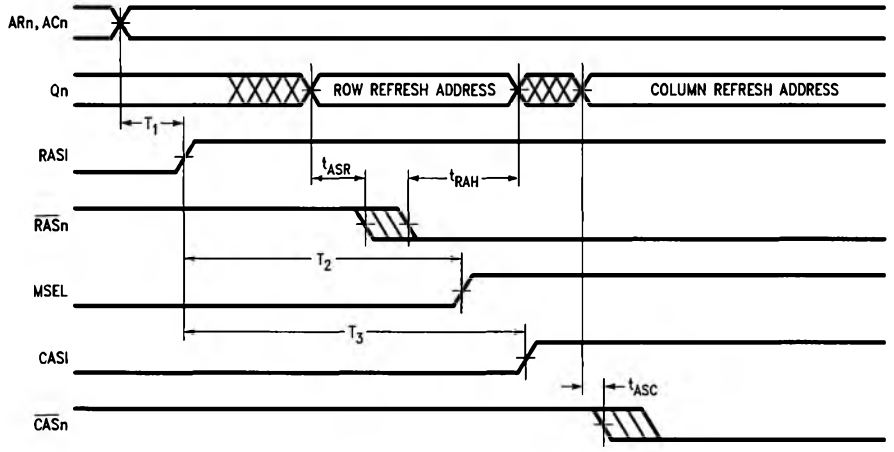


TL/F/9604–6

Note A: Guaranteed maximum difference between fastest RASI to $\overline{RAS}_n$ delay and the slowest A_n to Q_n delay on any single device.
Note B: Guaranteed maximum difference between fastest MSEL to Q_n delay and the slowest RASI to $\overline{RAS}_n$ delay on any single device.
Note C: Guaranteed maximum difference between fastest CASI to $\overline{CAS}_n$ delay and the slowest MSEL to Q_n delay on any single device.

FIGURE 2. Specifications Applicable to Memory Cycle Timing (MC_n = 1,0)

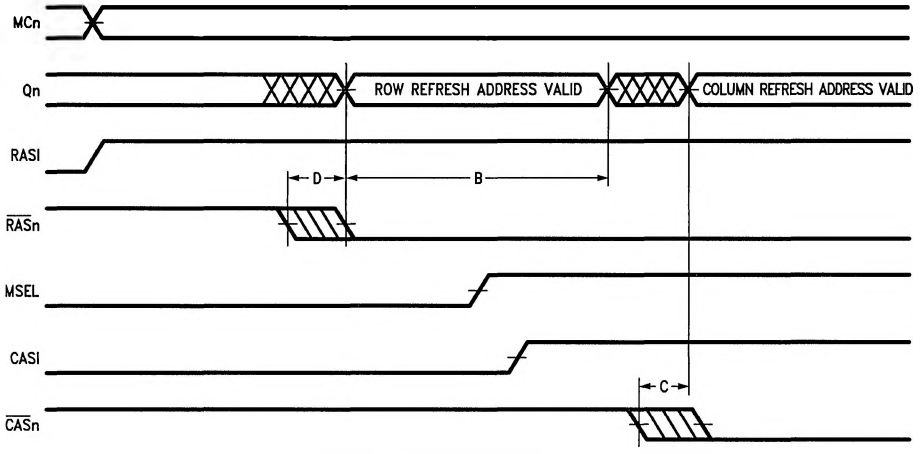
Memory Cycle Timing (Continued)



TL/F/9604–7

FIGURE 3. Desired System Timing

Refresh Cycle Timing

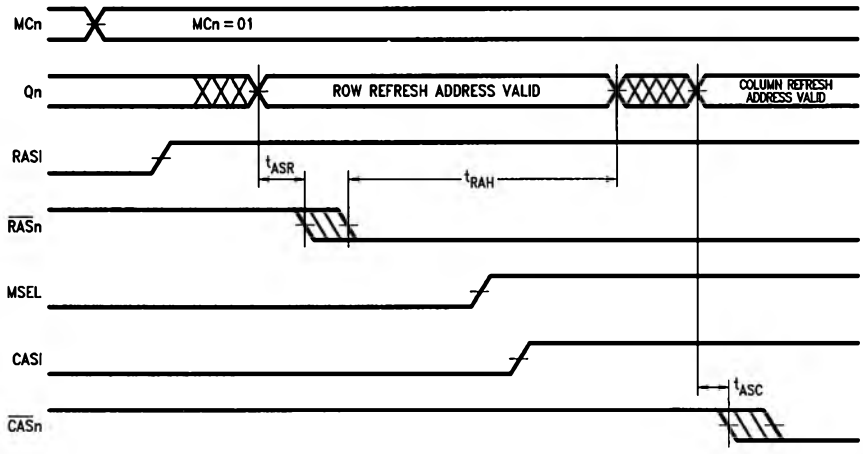


TL/F/9604–8

Note B: Guaranteed maximum difference between fastest MSEL to Q_n delay and the slowest RASI to $\overline{RAS}_n$ delay on any single device.
Note C: Guaranteed maximum difference between fastest CASI to $\overline{CAS}_n$ delay and the slowest MSEL to Q_n delay on any single device.
Note D: Guaranteed maximum difference between fastest RASI to $\overline{RAS}_n$ delay and the slowest MC_n to Q_n delay on any single device.

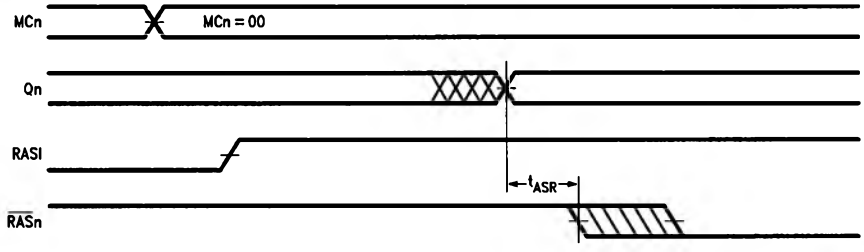
FIGURE 4. Specifications Applicable to Refresh Cycle Timing (MC_n = 00,01)

Refresh Cycle Timing (Continued)



TL/F/9604–9

FIGURE 5. Designed Timing—Refresh with Error Correction



TL/F/9604–10

FIGURE 6. Desired Timing—Refresh without Error Correction

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-State Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 1.0 mA
		54F 10% V_{CC}			0.8			I_{OL} = 12 mA
		74F 10% V_{CC}			0.5			I_{OL} = 1.0 mA
		74F 10% V_{CC}			0.8			I_{OL} = 12 mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Buss Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current				300	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current				300	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current				300	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	74F								Units
		$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A, V_{CC} =$ Com, $C_L = 50$ pF		$T_A, V_{CC} =$ Com, $C_L = 500$ pF*			
		Min	Typ	Max	Min	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation Delay AR to Q_n	3.0 3.0	7.0 7.0	11.0 11.0	2.5 2.5	12.0 12.0		19.0 22.0		ns
t_{PLH} t_{PHL}	Propagation Delay AC to Q_n	3.0 3.0	7.0 7.0	11.0 11.0	2.5 2.5	12.0 12.0		19.0 22.0		ns
t_{PLH} t_{PHL}	Propagation Delay RASI to $\overline{RAS}_n$	3.5 3.5	8.0 7.0	12.0 12.0	3.0 3.0	13.0 13.0		23.0 20.0		ns
t_{PLH} t_{PHL}	Propagation Delay CASI to $\overline{CAS}_n$	1.0 1.0	6.0 4.0	8.0 8.0	1.0 1.0	8.5 8.5		19.0 17.0		ns
t_{PLH} t_{PHL}	Propagation Delay MSEL to Q_n	3.0 3.0	9.0 8.0	13.0 13.0	2.5 2.5	14.0 14.0		24.0 21.0		ns
t_{PLH} t_{PHL}	Propagation Delay MC_n to Q_n	4.0 4.0	10.0 9.0	15.0 15.0	3.5 3.5	16.0 16.0		25.0 22.0		ns
t_{PLH} t_{PHL}	Propagation Delay MC_n to $\overline{RAS}_n$	3.5 3.5	11.0 8.0	17.5 17.5	3.0 3.0	18.5 18.5		24.0 22.0		ns
t_{PLH} t_{PHL}	Propagation Delay MC_n to $\overline{CAS}_n$	4.0 4.0	8.0 9.0	12.5 12.5	3.5 3.5	13.5 13.5		23.0 21.0		ns
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{RAS}_n$	4.0 4.0	10.0 9.0	15.0 15.0	3.5 3.5	16.0 16.0		25.0 24.0		ns
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{CAS}_n$	5.0 5.0	9.0 9.0	13.5 13.5	4.5 4.5	14.5 14.5		24.0 24.0		ns
t_{PLH} t_{PHL}	Propagation Delay LE to Q_n	3.5 3.5	8.0 7.0	12.0 12.0	3.0 3.0	13.0 13.0		23.0 22.0		ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CS}$ to Q_n	3.0 3.0	10.0 8.0	14.5 14.5	3.0 3.0	15.5 15.5		25.0 23.0		ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CS}$ to $\overline{RAS}_n$	3.5 3.5	8.0 8.0	13.0 13.0	3.0 3.0	14.0 14.0		23.0 23.0		ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CS}$ to $\overline{CAS}_n$	4.0 4.0	8.0 8.0	11.5 11.5	3.5 3.5	12.5 12.5		23.0 23.0		ns
t_{PLH} t_{PHL}	Propagation Delay SEL_n to $\overline{RAS}_n$	4.0 4.0	9.0 8.0	15.5 15.5	3.5 3.5	16.0 16.0		24.0 23.0		ns
t_{PLH} t_{PHL}	Propagation Delay SEL_n to $\overline{CAS}_n$	4.5 4.5	9.0 9.0	14.5 14.5	4.0 4.0	15.5 15.5		24.0 24.0		ns

*These values are given for typical derivative with a 500 pF load; these are not guaranteed specifications.

AC Electrical Characteristics

Symbol	Parameter	74F					Units
		$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			$T_A, V_{CC} = Com$ $C_L = 50\ pF$		
		Min	Typ	Max	Min	Max	
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Q_n	1.0 1.0	5.0 4.0	9.5 9.5	1.0 1.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Q_n	1.0 1.0	5.0 6.0	9.5 9.5	1.0 1.0	10.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to $\overline{RAS}_n$	1.0 1.0	5.0 4.0	9.5 9.5	1.0 1.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to $\overline{RAS}_n$	1.0 1.0	5.0 6.0	9.5 9.5	1.0 1.0	10.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to $\overline{CAS}_n$	1.0 1.0	5.0 4.0	9.5 9.5	1.0 1.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to $\overline{CAS}_n$	1.0 1.0	5.0 6.0	9.5 9.5	1.0 1.0	10.0 10.0	ns

AC Operating Requirements

Symbol	Parameter	74F				Units
		$T_A = +25°C$ $V_{CC} = +5.0V$		$T_A, V_{CC} = Com$		
		Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n to LE	5.0 5.0		5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n to LE	5.0 5.0		5.0 5.0		ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW SEL to LE	5.0 5.0		5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW SEL to LE	5.0 5.0		5.0 5.0		ns
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW $\overline{CAS}_n$, $\overline{RAS}_n$	15.0 15.0		15.0 15.0		ns
t_{skew}	Q_n to $\overline{CAS}_n$, $\overline{RAS}_n$	10.0		10.0		ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows: