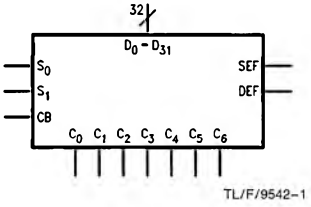
National Semiconductor

54F/74F420
Parallel Check Bit/Syndrome Bit Generator

General Description

The 'F420 is a parallel check bit/syndrome bit generator. The 'F420 utilizes a modified hamming code to generate 7 check bits from a 32-bit dataword, in 15 ns, when operated in the check bit generate mode. When operated in the syndrome generate mode, the check bits and data bits read from memory are utilized in a parity summer to generate syndrome bits upon error detection. The maximum error count detectable is 2. A single error detect can occur in 18 ns; a double error detect in 22 ns. The syndrome bit generation can be output in 15 ns (maximum).

Logic Diagram



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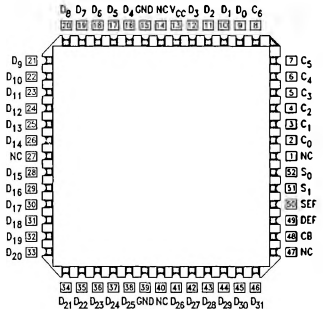
Connection Diagrams

Pin Assignment for LCC and PCC



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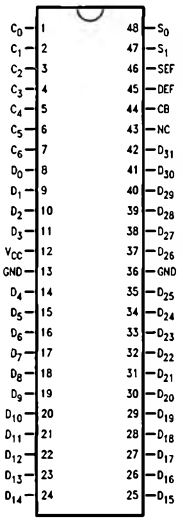
Pin Assignment for DIP and Flatpak



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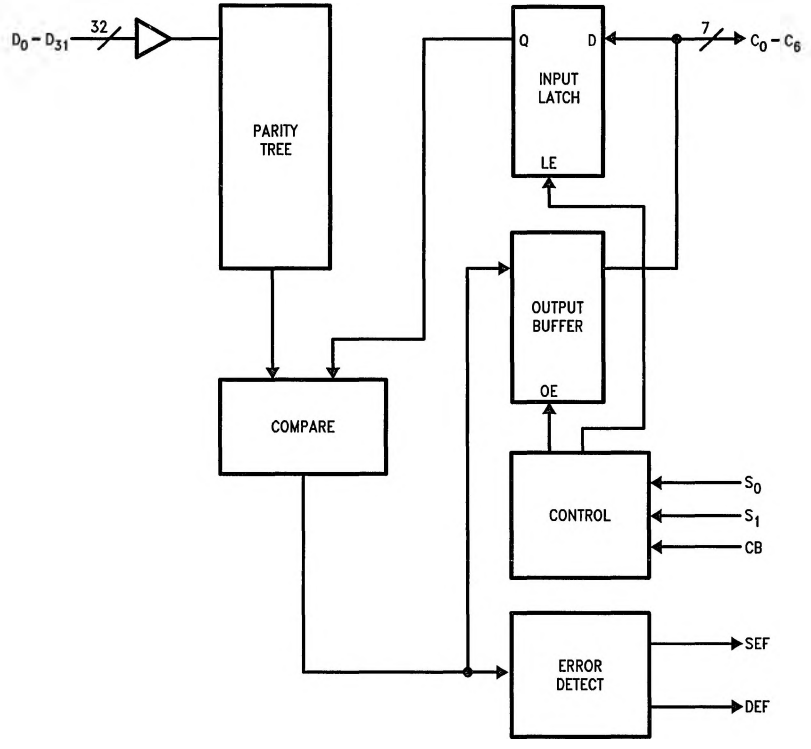
Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
C_0–C_6	Check Bit/Syndrome Bus Inputs/ Outputs	3.5/1.083 150/40 (33.3)	70 μA/−0.65 mA −3 mA/24 mA (20 mA)
D_0–D_{31}	Data Bit Bus	1.0/1.0	20 μA/−0.6 mA
CB	Check Bit Control	1.0/1.0	20 μA/−0.6 mA
DEF	Double Error Flag	50/33.3	−1 mA/20 mA
SEF	Single Error Flag	50/33.3	−1 mA/20 mA
S_0, S_1	Mode Control	1.0/1.0	20 μA/−0.6 mA

Function Table

Memory Cycle	Function	Control S_1	Control S_0	Check Bit	CB Control I/O	Error Flags SEF	Error Flags DEF
Write	Generate Check Bits	L	L	Output Check	L	H	H
Read	Read & Flag	H	L	Input	H	Enabled	
Read	Latch Check Bits	H	H	Inputs	H	Enabled	
Read	Output Syndrome Bits	H	H	Output Syndrome Bits	L	Enabled	
Diagnostics	Input Diagnostic Data Word	H	H	Latched Check Outputs High-Z	H	Enabled	
Diagnostics	Input Diagnostic Data Word	L	H	Output Latched Check Bits	L	Enabled	
Diagnostics	Input Diagnostic Data Word	H	H	Output Syndrome Bits	L	Enabled	

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA, D_n, CB, S_0, S_1
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA (All Outputs)
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA (C_0–C_6)
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA (All Outputs)
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA (C_0–C_6)
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA (All Outputs)
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA (C_0–C_6)
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA (All Outputs)
		74F 10% V_{CC}			0.5			I_{OL} = 20 mA (DEF, SEF)
		74F 10% V_{CC}			0.5			I_{OL} = 24 mA (C_0–C_6)
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 1.50 mV All Other Pins Grounded
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)				1.0	mA	Max	V_{IN} = 5.5V (C_0–C_6)
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (D_n, CB, S_0, S_1)
I_{IH} + I_{OZH}	Output Leakage Current				70	μA	Max	V_{OUT} = 2.7V (C_0–C_6)
I_{IL} + I_{OZL}	Output Leakage Current				−650	μA	Max	V_{OUT} = 0.5V (C_0–C_6)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current				130	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current				130	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current				130	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			54F $T_A, V_{CC} = Mil$ $C_L = 50\ pF$		74F $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	5.0		20.0			5.0	22.0	ns
t_{PHL}	D_n to C_n	5.0		17.0			5.0	19.0	
t_{PLH}	Propagation Delay	5.0		20.0			5.0	22.0	ns
t_{PHL}	D_n/C_n to SEF	4.0		16.0			4.0	18.0	
t_{PLH}	Propagation Delay	6.0		24.0			6.0	26.0	ns
t_{PHL}	D_n/C_n to DEF	5.0		21.0			5.0	22.0	
t_{PLH}	Propagation Delay	4.0		18.0			4.0	19.0	ns
t_{PHL}	S1 to C_n	3.0		13.0			3.0	14.0	
t_{PLH}	Propagation Delay	4.0		14.0			4.0	15.0	ns
t_{PHL}	S1 to SEF/DEF	3.0		9.0			3.0	10.0	
t_{PZH}	Output Enable Time	2.0		12.0			2.0	13.0	ns
t_{PZL}		2.0		11.0			2.0	12.0	
t_{PHZ}	Output Disable Time	1.0		7.5			1.0	8.0	
t_{PLZ}		1.0		7.5			1.0	8.0	

AC Operating Requirements

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} = Mil$		74F $T_A, V_{CC} = Com$		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$	Setup Time, HIGH or LOW	5.0				5.0		ns
$t_s(L)$	C_n to S_0	5.0				5.0		
$t_h(H)$	Hold Time, HIGH or LOW	5.0				5.0		ns
$t_h(L)$	C_n to S_0	5.0				5.0		
$t_w(L)$	Clock Pulse Width LOW	8.0				8.0		ns

Timing Waveforms

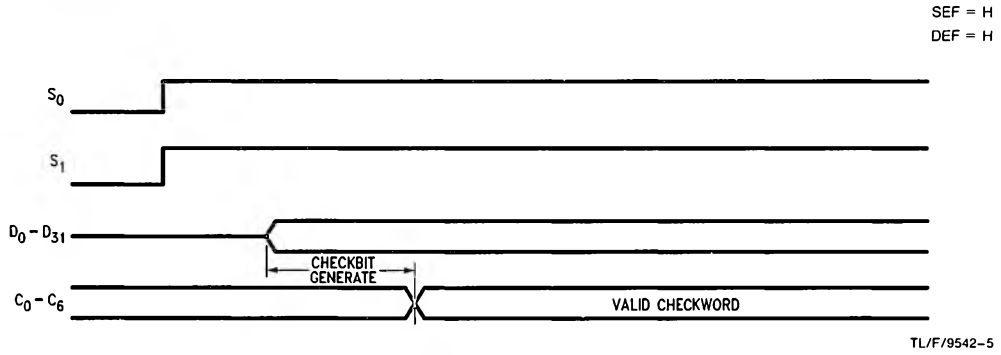

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FIGURE 420-a.

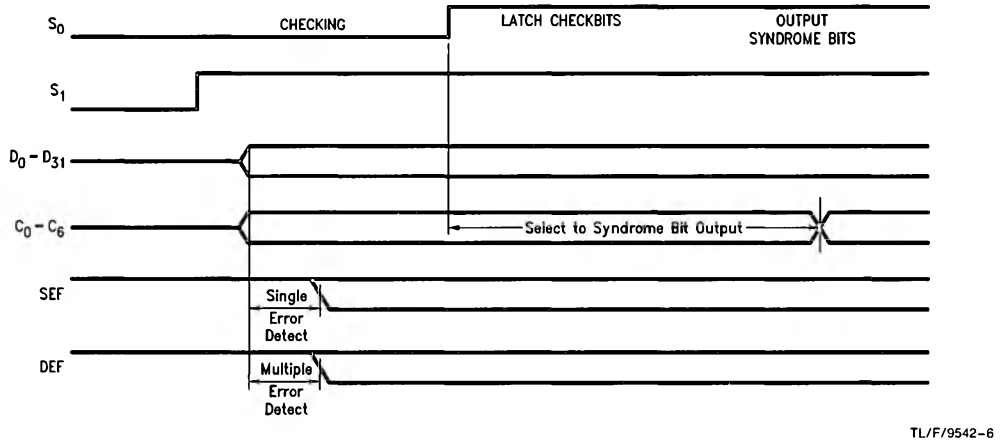

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FIGURE 420-b.

Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

74F 420 P C QR

Temperature Range Family
- 74F = Commercial
- 54F = Military
- 29F = Commercial or Military

Device Type

Package Code
- Q = Plastic Leaded Chip Carrier (PCC)

Special Variations
- QR = Commercial grade device with burn-in
- QB = Military grade with environmental and burn-in processing shipped in tubes

Temperature Range
- C = Commercial (0°C to +70°C)
- M = Military (−55°C to +125°C)