DATA SHEET

74F377A
Octal D-type flip-flop with enable

Product specification

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IC15 Data Handbook

Philips
Semiconductors

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Octal D-type flip-flop with enable 74F377A

FEATURES

- High impedance inputs for reduced loading (20µA in Low and High states)
- Ideal for addressable register applications
- Enable for address and data synchronization applications
- Eight edge–triggered D–type flip–flops
- Buffered common clock
- See 'F273A for Master Reset version
- See 'F373 for transparent latch version
- See 'F374 for 3–State version

DESCRIPTION

The 74F377A has 8 edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) input is Low.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The $\overline{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F377A	165MHz	29mA

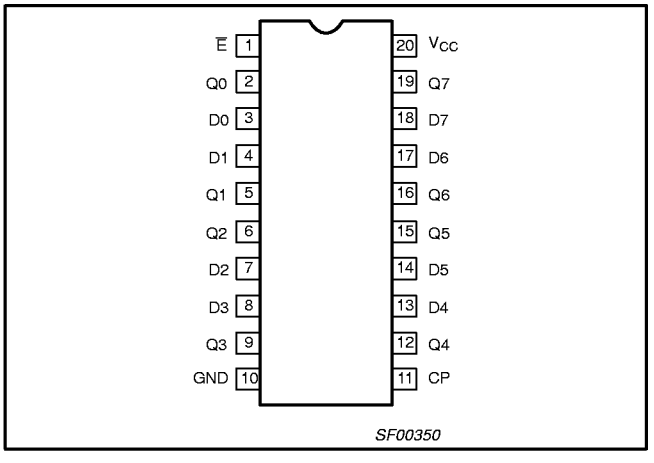
ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C	PKG. DWG. #
20–pin plastic DIP	N74F377AN	SOT146-1
20–pin plastic SOL	N74F377AD	SOT163-1

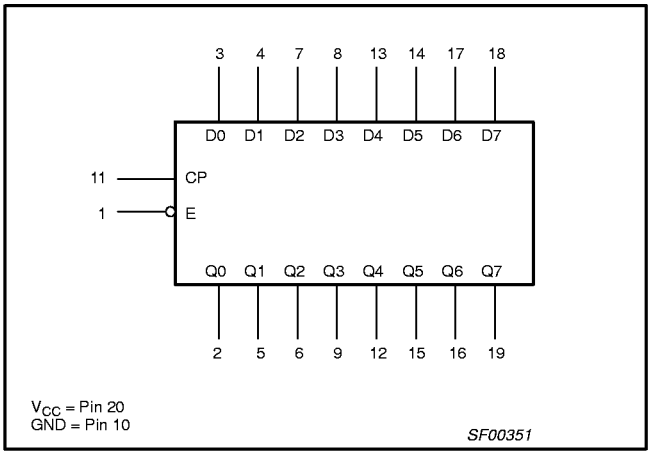
INPUT AND OUTPUT LOADING AND FAN–OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Data inputs	1.0/0.033	20µA/20µA
CP	Clock pulse input (active rising edge)	1.0/0.033	20µA/20µA
$\overline{E}$	Enable input (active–Low)	1.0/0.033	20µA/20µA
Q0 – Q7	Data outputs	50/33	1.0mA/20mA

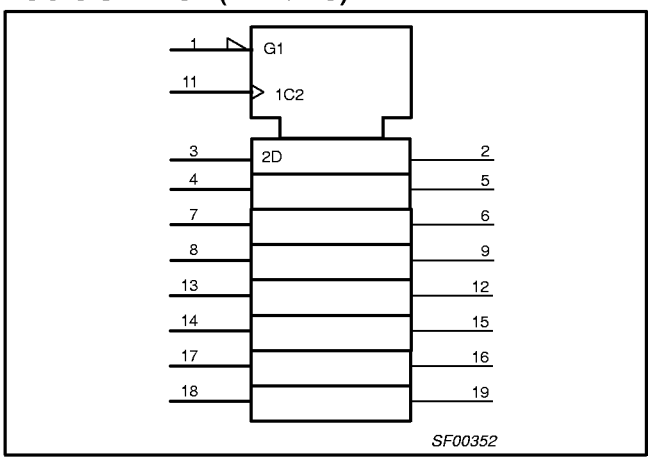
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

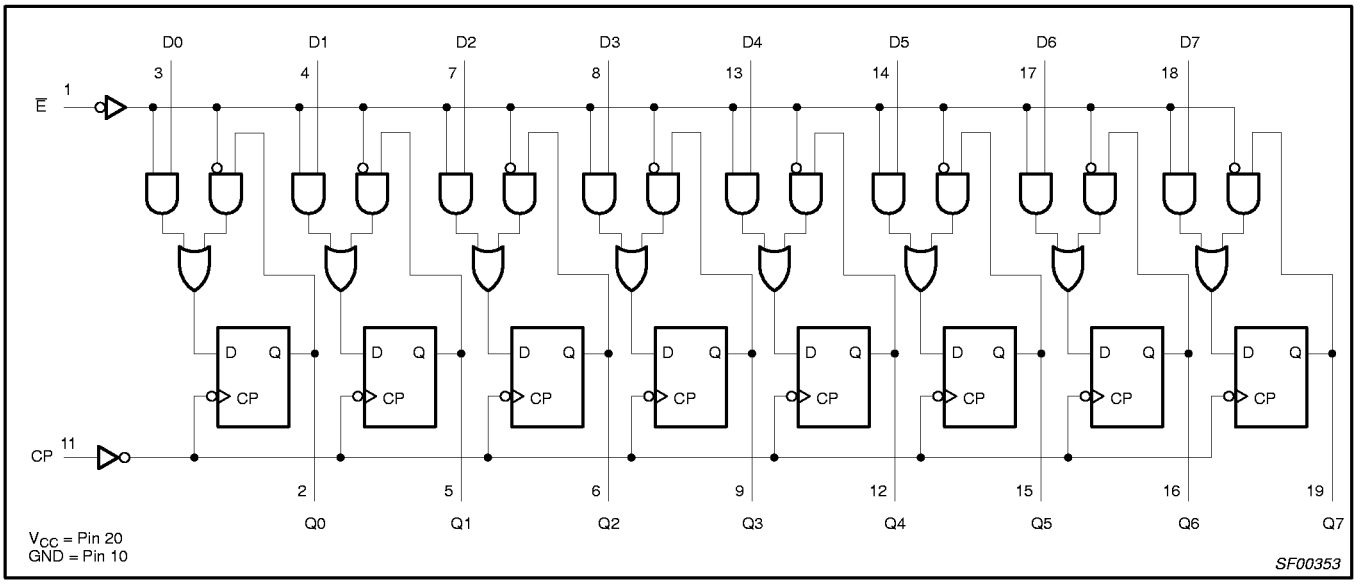


FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{E}$	CP	Dn	Qn	
l	↑	h	H	Load "1"
l	↑	l	L	Load "0"
h H	↑ X	X X	no change no change	Hold (do nothing)

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–1	mA
I_{OL}	Low–level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	$\overline{E}$ & CP inputs	V_{CC} = MIN, V_{IL} = 0.0V[3],	±10%V_{CC}	2.5			V
			V_{IH} = 4.5V[3], I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
		Other inputs	V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V				–20	µA
I_{OS}	Short circuit output current[4]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			27	40	mA
		I_{CCL}	V_{CC} = MAX			29	43	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. To reduce the effect of external noise during test. Special test conditions are not necessary for the '377A.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

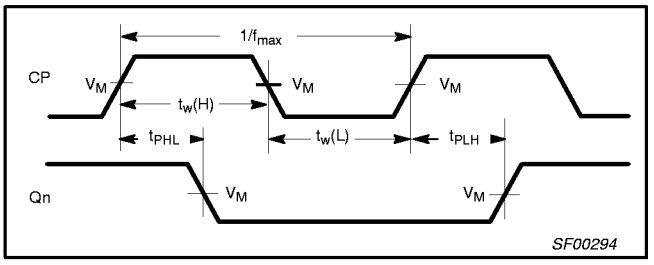
AC CHARACTERISTICS

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_{amb} =0°C to +70°C V_{CC} = +5.0V ±10% C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	150	165		120		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	3.0 4.5	5.0 6.5	8.0 9.0	2.5 4.0	9.0 10.5	ns

AC SETUP REQUIREMENTS

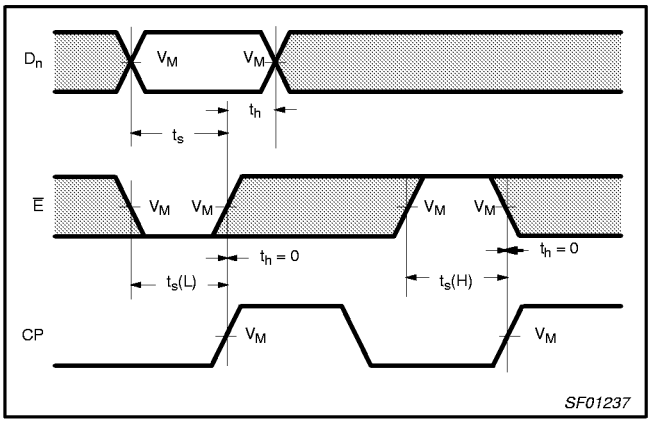
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ±10% C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low Dn to CP	2	2.5 2.5			2.5 2.5		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to CP	2	1.0 0.0			1.0 0.0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{E}$ to CP	2	3.0 4.0			3.0 4.5		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{E}$ to CP	2	0.0 0.0			0.0 0.0		ns
t_w(H) t_w(L)	Clock Pulse width High or Low	1	4.0 4.0			5.0 4.0		ns

AC WAVEFORMS



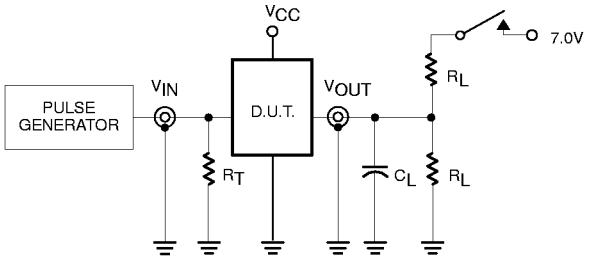
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 2. Data and Enable Setup and Hold Times

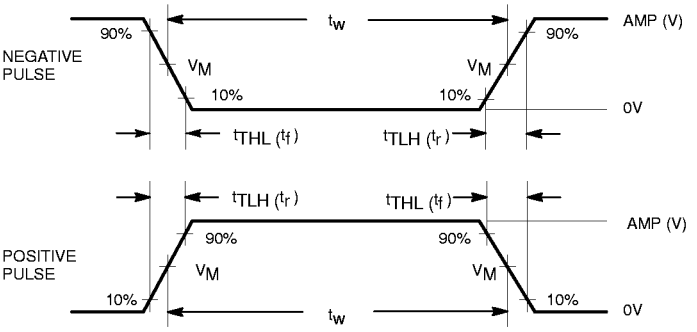
TEST CIRCUIT AND WAVEFORM



Test Circuit for Open Collector Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open



Input Pulse Definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

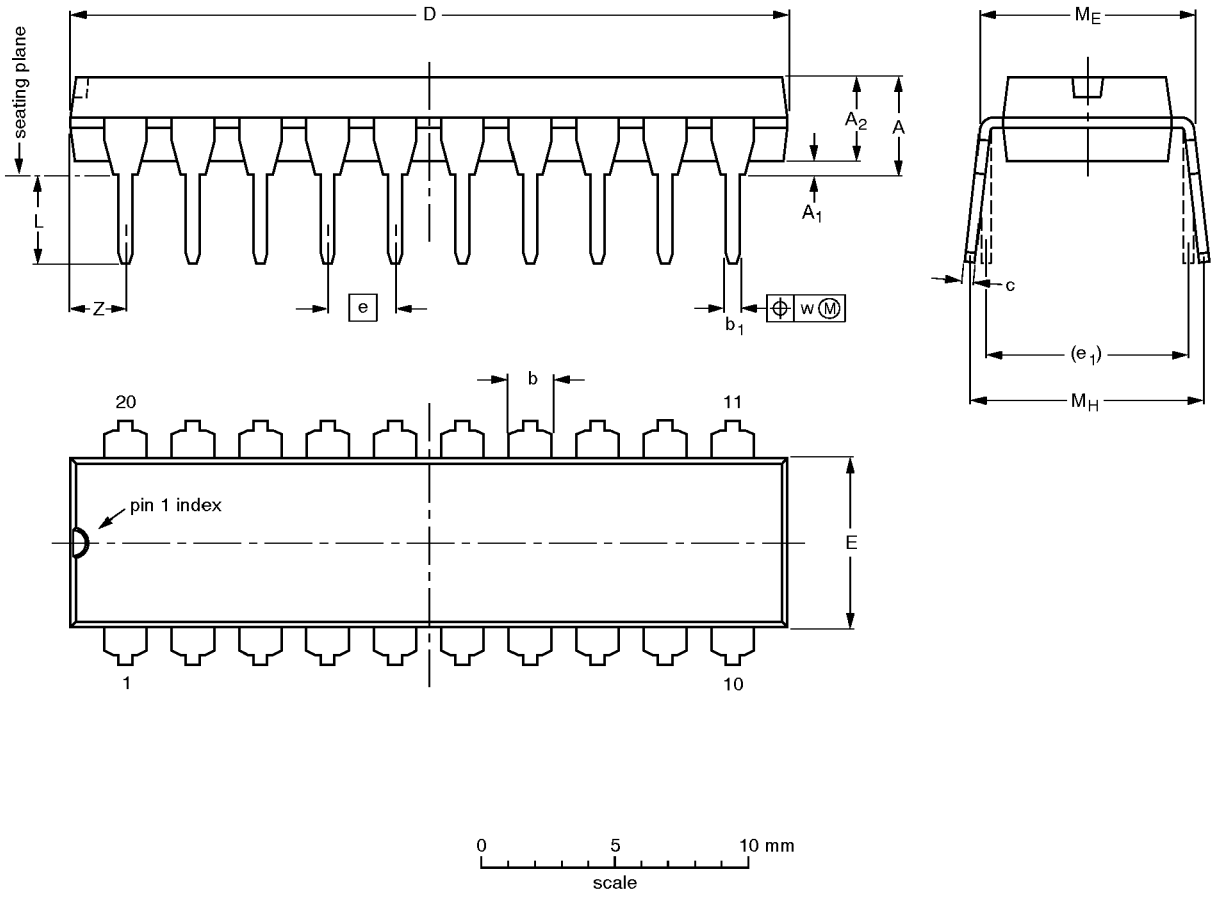
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

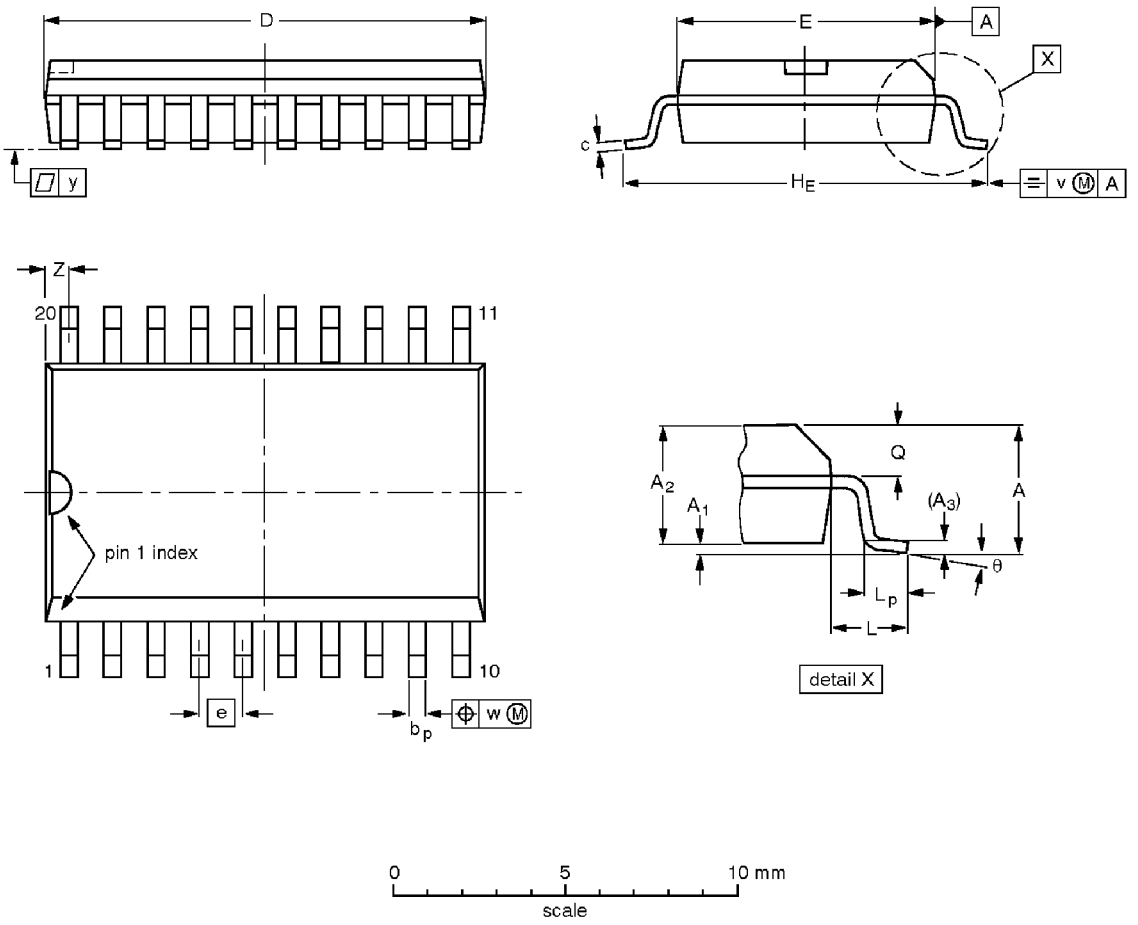
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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