National Semiconductor

PRELIMINARY

CGS64/74C800/801/802, CGS64/74CT800/801/802, CGS/74LCT800/801/802
Low Skew PLL 1-to-8 CMOS Clock Driver

General Description

These minimum skew clock drivers are designed for Clock Generation and Support (CGS) applications operating at high frequencies utilizing a phase lock loop. The phase lock loop allows for outputs to lock-on to either Synch_0 or Synch_1 inputs, which could be operating at different frequencies. This product is ideal for applications requiring clock synchronization and distribution of either on or off board components.

The PLL uses a counter and a digital to analog convertor for its charge pump and the loop filter and does NOT require any external components for the loop filter. This along with separate analog and digital power rails, helps to minimize the overall sensitivity of the part to noise. The VCO is optimized to operate from 10 MHz up to twice the operating frequency of the 2X output.

The eight outputs, O0–O7, are provided for large fanout applications requiring different phase/frequency clocks. The output buffer of the 800 option includes 5 drivers (O0–O4) with 500 ps skew across either rising or falling edges running at the same frequency as the input. Also included on the 800 option are, O5 which is 180 degrees out of phase output, O6 which is running at twice the input frequency, and O7 an in-phase divide-by-two clock output.

The 801 option has all the output (O0–O7) operating at the same frequency as the input (half the VCO frequency) with a skew of no more than 500 ps.

The 802 option's output buffer consists of two drivers running at twice the input frequency, two drivers at the same frequency, and two drivers at half the input frequency. The last two drivers are operating at 1/4 and 3/2 of the reference frequency (refer to the block diagram).

The Synch_0 and Synch_1 inputs are provided as two different sources for the input reference frequency and can be selected by the REF_SEL pin. These two inputs also can be used for any fault tolerant conditions by being at the same frequency.

The Feedback pin can be used for synchronizing the drivers to any selected output, or for synchronizing the drivers to any external signal.

Also provided is a reset circuitry to actively force the outputs to a low state. This is achieved by the RST pin (active low) which forces all the outputs to low.

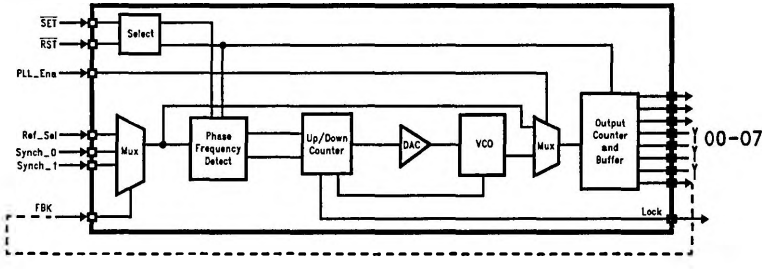
Another available feature is low frequency testing, which can be accomplished by disabling and by-passing the phase lock loop using the PLL_ENA pin. This pin causes the Synch_0 input to control the output counter.

A lock detect circuitry is also provided to determine the lock condition. This pin (LOCK) will remain low until the outputs and Synch Inputs are synchronized with the feedback signal. This pin can be used for wait or any interrupt states when the loops steady state phase or frequency lock is lost.

Features

- Guaranteed and tested:
  - 500 ps pin-to-pin skew (T_{OSHL} and T_{OSLH}) on 1X outputs
- Available in 3.3V and 5V options
- Output buffer of eight drivers for large fanout
- 10 MHz to 130 MHz output frequency
- NO LOOP FILTER COMPONENTS required for the PLL
- Motorola's PC88915 functional compatible (800 option)
- Outputs operating at 2X, 1X, 1X (bar), X/2, 3X/2, X/4 of the reference frequency for multi-frequency bus applications
- Two selectable glitch free reference clock available for test or fault tolerant conditions
- Open collector lock pin to enable cascading PLLs by wire-ORing them together
- Low frequency test mode by disabling the PLL
- Phase and frequency lock detect for power-up or interrupt and wait states
- Improved noise sensitivity and jitter performance
- Open drain lock indicator for ease of cascading
- Implemented on National's BCT 1.0 process
- Symmetric output current drive: +24/−24 mA I_{OH}/I_{OL}
- Industrial temperature of −40C to +85C
- 28-pin PCC for optimum skew performance
- Guaranteed 2 kV ESD protection

Block Diagram



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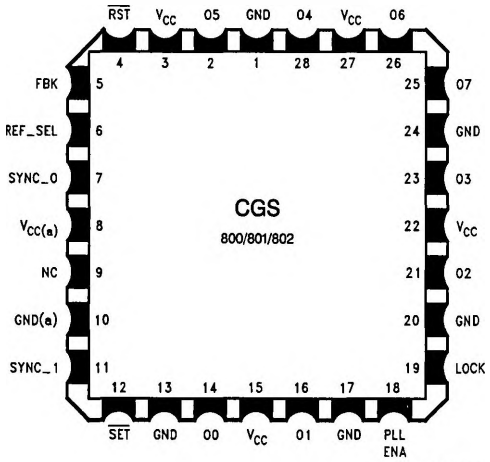
Connection Diagram

Pin Assignment for PLCC



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CGS800 Options Output Buffer

Pin Outputs	800	801	802
(14) O0	1X	1X	1X
(16) O1	1X	1X	1X
(21) O2	1X	1X	1X
(23) O3	1X	1X	1X
(28) O4	1X	1X	1/2X
(2) O5	1X (Bar)	1X	1/2X
(26) O6	2X	1X	1/4X
(25) O7	1/2X	1X	3/2X

Truth Table

Input						Output	
PLL ENA	REF SEL	S_0	S_1	SET	RESET	O	LOCK
L	X	X	X	L	L	L	L
L	X	X	X	L	H	L	L
L	X	X	X	H	L	L	L
L	L	⎍	X	H	H	⎍	H*
L	H	X	⎍	H	H	⎍	H*
H	L	⎍	X	H	H	⎍	L
H	H	X	⎍	H	H	⎍	L

*Phase, Frequency Locked State.

Pin Description PLCC Package

Pin	Name	Description
1	GND	Digital Ground
2	Output 5	Output
3	V_{CC}	Digital V_{CC}
4	Reset	Reset Active Low (Asynchronous)
5	Feedback	PLL Feed Back Path
6	Input Select	Reference Input Clock Select
7	Input 0	Clock 0 Input
8	Analog V_{CC}	Analog V_{CC}
9	N/C	No Connect
10	GND	Digital Ground
11	Input 1	Clock 1 Input
12	Set	Set Active Low (Asynchronous)
13	Analog GND	Analog Ground
14	Output 0	Output
15	V_{CC}	V_{CC}
16	Output 1	Output
17	GND	Ground
18	PLL Enable	PLL Enable for Test
19	LOCK	Lock
20	GND	Ground
21	Output 2	Output
22	V_{CC}	V_{CC}
23	Output 3	Output
24	GND	Ground
25	Output 7	Output
26	Output 6	Output
27	V_{CC}	V_{CC}
28	Output 4	Output

CGS64/74CT, C800/800/801/802 Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Voltage Diode Current (I_{IK})	
$V = -0.5V$	−20 mA
$V = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_O)	
$V = -0.5V$	−20 mA
$V = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +125°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
Ind.	−40°C to +85°C
Comm.	0°C to +70°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note: *The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter		Conditions	V_{CC}	V_{CC} = 4.5V to 5.5V, T_A = −40°C to +85°C			Units
					Min	Typ	Max	
V_{IH}	Minimum Input High Level Voltage	C800/801/802	V_{OUT} = 0.1V or V_{OUT} = V_{CC} − 0.1V	4.5 5.5	2.1 3.85	1.5 2.75		V
		CT800/801/802		4.5 5.5	2.0 2.0			
V_{IL}	Maximum Input Low Level Voltage	C800/801/802	V_{OUT} = 0.1V or V_{OUT} = V_{CC} − 0.1V	4.5 5.5		1.5 2.75	0.9 1.65	V
		CT800/801/802		4.5 5.5			0.8 0.8	
V_{OH}	Minimum Output High Level Voltage	C800/801/802	I_{OUT} = −50 μA	4.5 5.5	4.4 5.4	4.4 5.4		V
		CT800/801/802		4.5 5.5	4.4 5.4	4.4 5.4		
		C800/801/802	I_{OH} = −24 mA	4.5 5.5	3.7 4.7	3.76 4.76		V
		CT800/801/802		4.5 5.5	3.7 4.7	3.76 4.76		
V_{OL}	Maximum Output Low Level Voltage	C800/801/802	I_{OUT} = −50 μA	4.5 5.5		0.1 0.1	0.1 0.1	V
		CT800/801/802		4.5 5.5		0.1 0.1	0.1 0.1	
		C800/801/802	I_{OL} = 24 mA	4.5 5.5		0.1 0.1	0.44 0.44	V
		CT800/801/802		4.5 5.5		0.1 0.1	0.44 0.44	
I_{IN}	Leakage Current		CT800/801/802 C800/801/802	V_{IN} = V_{CC}, GND	5.5	−1.0		+0.1	μA
I_{CC}	Maximum Supply Current	Analog	CT800/801/802 C800/801/802	V_{IN} = V_{CC}, GND	5.5			50.0 50.0	mA
		Digital	CT800/801/802 C800/801/802		5.5			1.0 1.5	

CGS74LCT, 800/801/802

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage Diode Current (I_{IK})	
$V = -0.5V$	−20 mA
$V = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_O)	
$V = -0.5V$	−50 mA
$V = V_{CC} + 0.5V$	+50 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +125°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0 to V_{CC}
Operating Temperature (T_A)	−0°C to +70°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V, 3.6V	125 mV/ns

Note: *The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 3.3V, T_A = 25°C

Symbol	Parameter		Conditions	V_{CC}	V_{CC} = 3.3V to 3.6V, T_A = 0°C to +70°C			Units
					Min	Typ	Max	
V_{IH}	Minimum Input High Level Voltage	LCT800/801/802	V_{OUT} = 0.1V or V_{OUT} = V_{CC} − 0.1V	3.3	2.0			V
V_{IL}	Maximum Input Low Level Voltage	LCT800/801/802	V_{OUT} = 0.1V or V_{OUT} = V_{CC} − 0.1V	3.3			0.8	V
V_{OH}	Minimum Output High Level Voltage	LCT800/801/802	I_{OUT} = −50 μA	3.3	V_{CC} −0.2			V
		LCT800/801/802	I_{OH} = −24 mA	3.3	2.4			V
V_{OL}	Maximum Output Low Level Voltage	LCT800/801/802	I_{OUT} = −50 μA	3.3			0.2	V
		LCT800/801/802	I_{OL} = 24 mA	3.3			0.5	V
I_{IN}	Leakage Current	LCT800/801/802	V_{IN} = V_{CC}, GND	3.6	−1.0		+0.1	μA
I_{CC}	Maximum Supply Current, Analog	LCT800/801/802	V_{IN} = V_{CC}, GND	3.6			50.0 50.0	mA
	Maximum Supply Current, Digital	LCT800/801/802		3.6			1.0 1.5	mA

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter			V_{CC} = 4.5V to 5.5V T_A = −40°C to +85°C C_L = 50 pF R_L = 500Ω			Units	Notes
				Min	Typ	Max		
t_r	Output Rise	0.8V to 2.0V				1.5	ns	
		0.2 V_{CC} to 0.8 V_{CC}				2.5		
t_f	Output Fall	0.8V to 2.0V				1.5	ns	
		0.2 V_{CC} to 0.8 V_{CC}				2.5		
t_{SKEW}	Maximum Edge-to-Edge Output Skew	+ to + edges − to − edges + to − edges	CGS800			500 500 750	ps	(Note 1)
		All edges	CGS801			500	ps	(Note 2)
		+ to + edges − to − edges + to − edges	CGS802			500 500 750	ps	(Note 3)
$t_{PULSE\ WIDTH}$	Output Pulse Width from Synch_0 or Synch_1 in Test Mode			Period/2 ±0.5		Period/2 ±0.5	ns	
$t_{PROP-DELAY}$	Synch to Feedback Delay Master Set/Reset to Q Master Set to Lock Master Reset to Lock PLL Enable to Lock Synch Loss to Lock			 8 Cycles		0.5 8.0 TBD TBD 5.0 16 Cycles + 10 ns	ns	(Note 4)
t_{LOCK}	Time to Lock the Output to the Synch Input					10.0	ms	(Note 5)
$t_{RECOVERY}$	Reset Recovery to Synch_0/1			9.0			ns	(Note 6)
t_{WIDTH}	Set/Reset Input Pulse Width Synch_0/1 Minimum Pulse Width			5.0 3.0			ns	(Note 7)
t_{CYCLE}	Input Duty Cycle			25%		75%	ns	(Note 8)
f_{max}	Output Operating Frequency			10.0		130.0	MHz	(Note 9)
Jitter	Output Jitter					500	ps	(Note 10)
C_{IN}	Input Capacitance				5.0		pF	
C_{PD}	Power Dissipation Capacitance				50.0		pF	

CGS74LCT800/801/802

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 3.3V, T_A = 25°C

Symbol	Parameter			V_{CC} = 3.0V to 3.6V T_A = −40°C to +85°C C_L = 50 pF R_L = 500Ω			Units	Notes
				Min	Typ	Max		
t_r	Output Rise	0.8V to 2.0V				1.5	ns	
		0.2 V_{CC} to 0.8 V_{CC}				2.5		
t_f	Output Fall	0.8V to 2.0V				1.5	ns	
		0.2 V_{CC} to 0.8 V_{CC}				2.5		
t_{SKEW}	Maximum Edge-to-Edge Output Skew	+ to + edges − to − edges + to − edges	CGS800			500–750 500–750 750	ps	(Note 1)
		All edges	CGS801			500–750	ps	(Note 2)
		+ to + edges − to − edges + to − edges	CGS802			500–750 500–750 750	ps	(Note 3)
$t_{PULSE\ WIDTH}$	Output Pulse Width from Synch_0 or Synch_1 in Test Mode			Period/2 ±0.5		Period/2 ±0.5	ns	
$t_{PROP-DELAY}$	Synch to Feedback Delay Master Set/Reset to Q Master Set to Lock Master Reset to Lock PLL Enable to Lock Synch Loss to Lock			 8 Cycles		0.5 8.0 TBD 5.0 16 Cycles + 10 ns	ns	(Note 4)
t_{LOCK}	Time to Lock the Output to the Synch Input					10.0	ms	(Note 5)
$t_{RECOVERY}$	Reset Recovery to Synch_0/1			9.0			ns	(Note 6)
t_{WIDTH}	Set/Reset Input Pulse Width Synch_0/1 Minimum Pulse Width			5.0 3.0			ns	(Note 7)
t_{CYCLE}	Input Duty Cycle			25%		75%	ns	(Note 8)
f_{max}	Output Operating Frequency			10.0		100.0	MHz	(Note 9)
Jitter	Output Jitter			−250		+250	ps	(Note 10)
C_{IN}	Input Capacitance				5.0		pF	
C_{PD}	Power Dissipation Capacitance				50.0		pF	

AC Electrical Characteristics (Continued)

Note 1: Skew is measured at 50% of output level. For the case of 800 rising edge to rising edge, reflects output to output skew between Q0–Q4 and the rising output of Q7.

For falling edges it reflects the skew from output to output between Q0–Q4.

Also rising to falling skew reflects the output skew between the positive edges of 2XQ, Q0–Q4 and Q/2 with the negative edge of Q5. See *Figure 1*.

Note 2: For CGS801 skew is measured at the 50% level of the rising or falling edge transitions across outputs from Q0–Q7. See *Figure 2*.

Note 3: Skew is measured at 50% of output level. For the case of 802 rising edge to rising edge, reflects output to output skew between Q0–Q6.

For falling edges it reflects the skew from output to output between Q0 and Q1 or Q2 and Q3 or Q4 and Q5.

Also rising to falling skew reflects the output skew between the positive edges of 2XQ, Q0–Q4 and Q/2 with the negative edge of Q5. See *Figure 3*.

Note 4: Output pulse width is measured at $V_{CC}/2$. This parameter refers to a long term jitter versus period to period jitter and is guaranteed by design only. (Also refer to Note 10.)

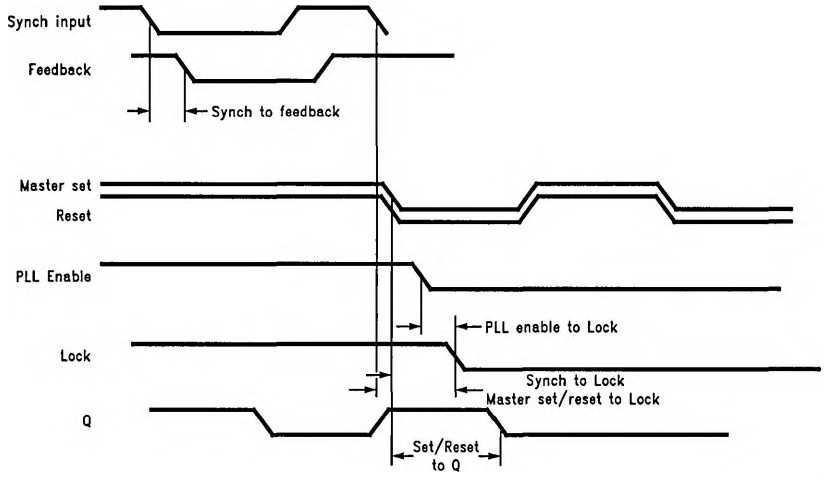
Note 5: Synch to feedback delay measures the delay (hold) required for the feedback to either of the synch inputs.

Master set or Reset propagation delays measures from 50% of the input to 50% of the output levels the amount of time for the output to transition to low state from its locked state.

Master set or Reset to Lock is measured from 50% of the input to 50% of the output. It is the amount of time required for the chip to acknowledge its reset condition via the lock pin.

PLL enable to Lock propagation delay is also measured from 50% of the input to 50% of the output level and it reflects the amount of time again to the lock pin to acknowledge its loss of lock for test chip enabling.

Synch loss to lock is also measured from 50% to 50% of the input/output levels and is the amount of time required for the chip to detect a loss of input signal. It can be used for fault tolerant applications. See figure below.



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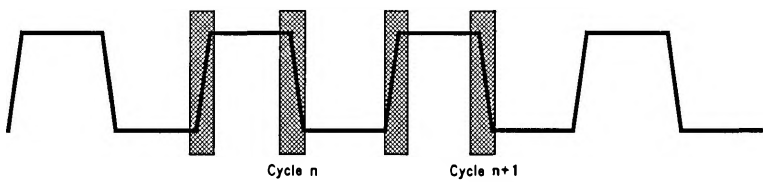
Note 6: Reset recovery time is measured from the rising edge of the reset pin to falling edge of the synch pin.

Note 7: t_{WIDTH} is measured at maximum V_{CC} and at 1.5V input levels.

Note 8: Input duty cycle is twice the reciprocal of the f_{max}. This reflects the maximum duty cycle allowed as an input to these devices. The actual duty cycle is not relevant since the part internally operates on a negative transition and performs a divide-by-two function.

Note 9: f_{max} is the maximum output frequency allowed. It represents the 2X outputs on the 800 and the 802 options, while f_{max} is for the X output on the 801.

Note 10: Jitter parameter is characterized and is guaranteed by design only. It measures the uncertainty of either the positive or the negative edge compared to its previous cycle. It is also measured at output levels of $V_{CC}/2$. Refer to figure below for further explanation.



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P(n) − P(n + 1) = ±250 ps for Either The Rising Or Falling Edge

AC Electrical Characteristics (Continued)

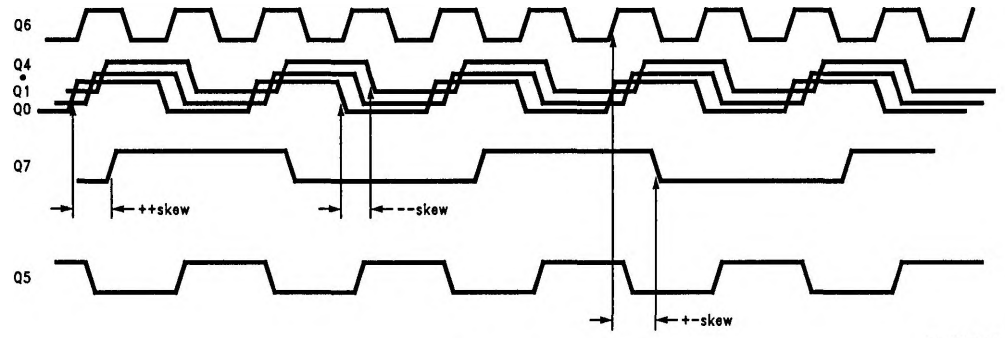

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FIGURE 1. CGS800

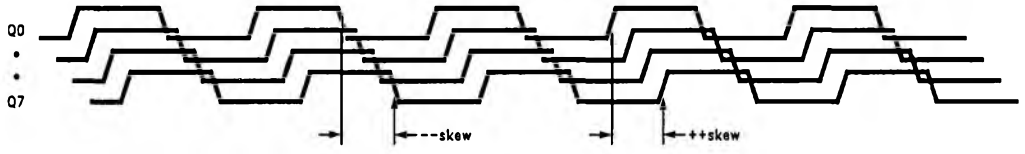

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FIGURE 2. CGS801

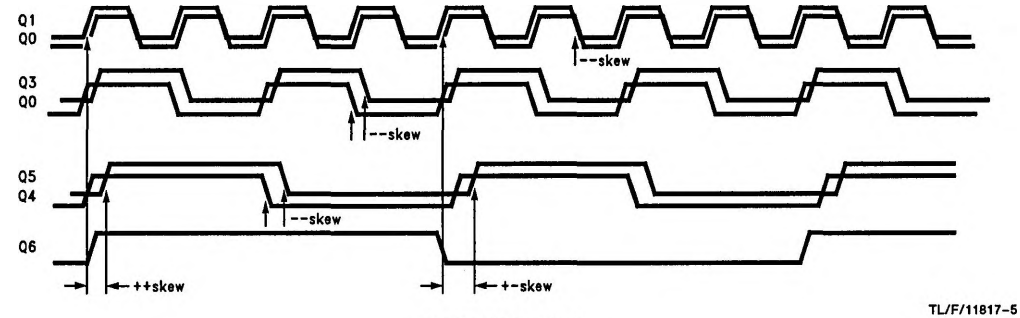

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FIGURE 3. CGS803

Typical Applications

The following represents some of the applications for the CGS800 and it options. In these applications 800/801/802 are used to generate and distribute clock signals for components that need synchronization.

The 802 has a 3/2 output which can be used to generate 50 MHz signals given a source of 33 MHz.

The next example also depicts typical usage for these products. The cache module could be either fully synchronized or non-fully synchronized.

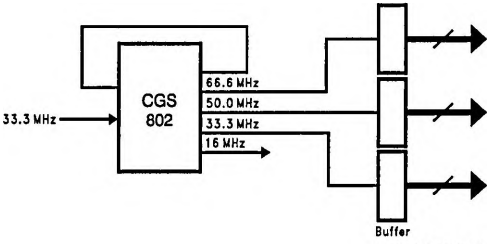
In the latter case the MBC runs at the same frequency as the CPU and so do the cache controller as well as the SRAMs. This can be achieved by providing a 1 to n clock driver/buffer to fanout the required input clock signals across the module. For the non-fully synchronized case, since the MBC and SRAMs as well as the controller are running at half the frequency of the CPU, the required buffer can be eliminated since the 800 and its options provide enough outputs to drive the required components.

Also another ideal application for these products are clock distribution across backplanes. Since these products include a digital PLL, the noise sensitivity is relatively less than their analog counterparts. This enables transmission of the required signal at half the frequency across the backplane. The outputs then can be synchronized together given a feedback reference signal.

The total skew for all the above applications must be calculated by adding the pin-to-pin skew of the 800 series to the part-to-part and the pin-to-pin of any required buffers.

$$t_{SKEW\ (tot)} = t_{OSHL/HL(PLL)} + (t_{pv} + t_{OSHL/HL})\ (Buffer)$$

Also to ensure jitter free operation of the PLL clock drivers, both ground and V_{CC} chokes must be used along with a bypass capacitor between the analog ground plane and the board power plane. A capacitor of 0.1 μF is recommended for bypassing, while the inductor size depends on the frequency of the operation as well as the induced noise frequency(ies) from both the power and the analog planes.



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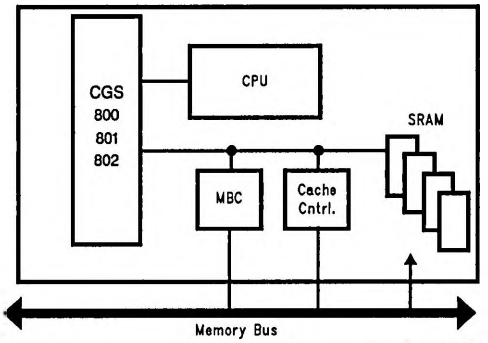

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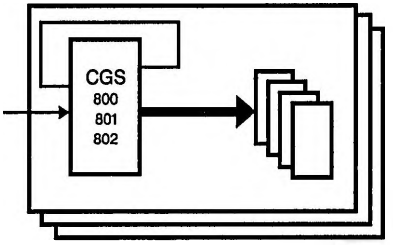

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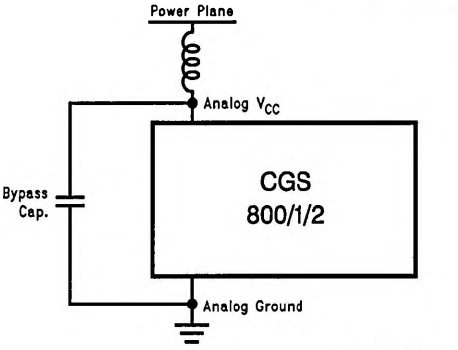

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Applications Requiring Cascading Phase Lock Loops

Due to the accumulation of noise, it is not recommended to cascade phase lock loops. However cascading phase lock loops can be beneficial in large clock trees due to the elimination of part to part skew.

CGS800 series clock drivers are less sensitive to noise since they do not require any external components for the loop filter. Additionally the lock indicator being an open drain output, allows this pin to be wired-OR to enable the system to achieve lock state once all the PLLs have acquired a lock on the frequency.

In the diagram below one such application is depicted. The source frequency is the incoming signal. This signal which is often generated from a crystal oscillator is the base frequency of the system. The PLL1, while generating a bank of outputs, bank 1, has also generated the source input signals for PLLs 3 and 4. While PLL3's outputs have generated the reference input frequency for the PLL2.

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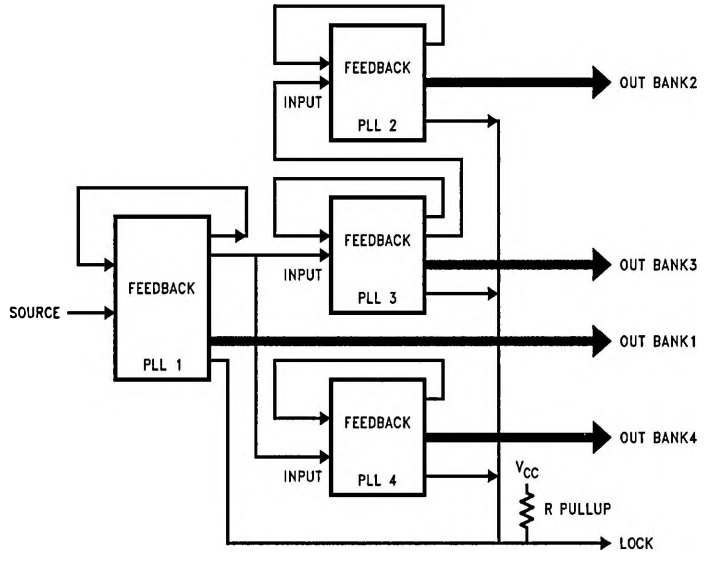

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