



54AC/74AC377 • 54ACT/74ACT377

Octal D Flip-Flop with Clock Enable

General Description

The 'AC/'ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (CE) is LOW.

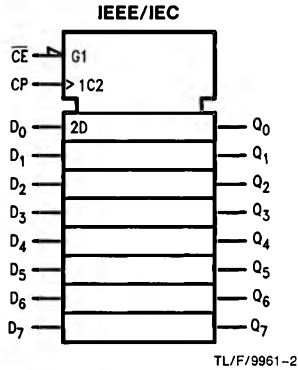
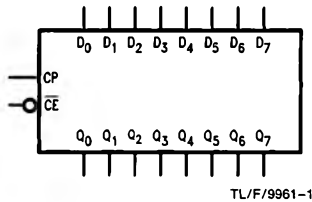
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The CE input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Features

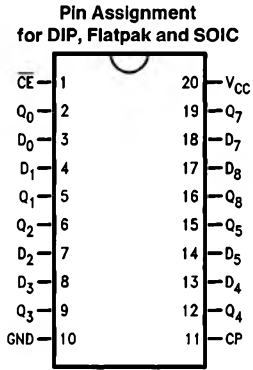
- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- Outputs source/sink 24 mA
- See '273 for master reset version
- See '373 for transparent latch version
- See '374 for TRI-STATE® version
- 'ACT377 has TTL-compatible inputs
- Standard Military Drawing (SMD)
 - 'AC377: 5962-88702
 - 'ACT377: 5962-87697

Ordering Code: See Section 8

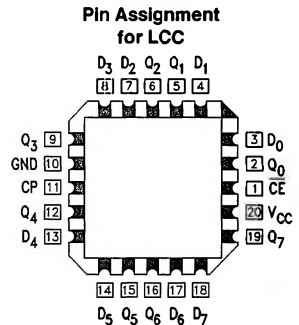
Logic Symbols






Connection Diagrams




Pin Names	Description
D ₀ -D ₇	Data Inputs
CE	Clock Enable (Active LOW)
Q ₀ -Q ₇	Data Outputs
CP	Clock Pulse Input

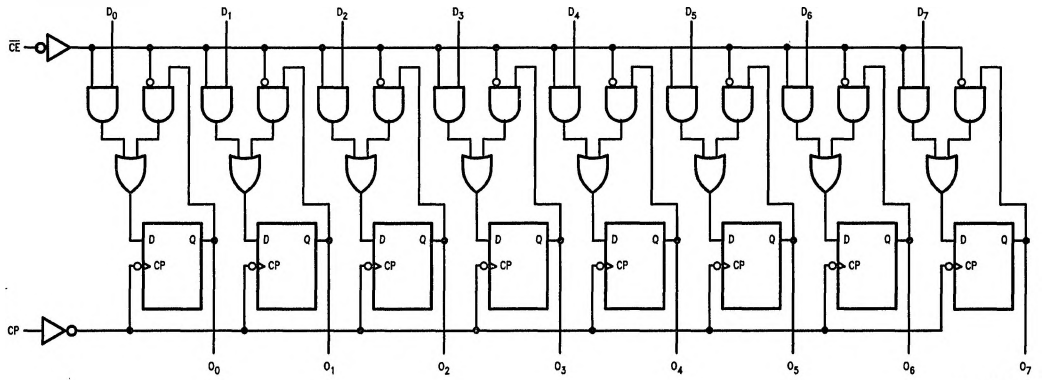


Mode Select-Function Table

Operating Mode	Inputs			Outputs
	CP	\overline{CE}	D_n	Q_n
Load '1'		L	H	H
Load '0'		L	L	L
Hold (Do Nothing)		H	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})		2.0V to 6.0V
'AC		4.5V to 5.5V
'ACT		
Input Voltage (V_I)		0V to V_{CC}
Output Voltage (V_O)		0V to V_{CC}
Operating Temperature (T_A)		-40°C to +85°C
74AC/ACT		-55°C to +125°C
54AC/ACT		
Minimum Input Edge Rate ($\Delta V/\Delta t$)		
'AC Devices		
V_{IN} from 30% to 70% of V_{CC}		
V_{CC} @ 3.3V, 4.5V, 5.5V		125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)		
'ACT Devices		
V_{IN} from 0.8V to 2.0V		
V_{CC} @ 4.5V, 5.5V		125 mV/ns

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC			54AC			74AC			Units	Conditions
			$T_A = +25^\circ\text{C}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$				
			Typ	Guaranteed Limits									
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	2.1	V	V _{OUT} = 0.1V or $V_{CC} - 0.1V$				
		4.5	2.25	3.15	3.15	3.15	3.15						
		5.5	2.75	3.85	3.85	3.85	3.85						
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	0.9	V	V _{OUT} = 0.1V or $V_{CC} - 0.1V$				
		4.5	2.25	1.35	1.35	1.35	1.35						
		5.5	2.75	1.65	1.65	1.65	1.65						
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$				
		4.5	4.49	4.4	4.4	4.4	4.4						
		5.5	5.49	5.4	5.4	5.4	5.4						
		3.0		2.56	2.4	2.46	2.46	V	* $V_{IN} = V_{IL}$ or V_{IH} -12 mA I_{OH} -24 mA -24 mA				
		4.5		3.86	3.7	3.76	3.76						
		5.5		4.86	4.7	4.76	4.76						
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$				
		4.5	0.001	0.1	0.1	0.1	0.1						
		5.5	0.001	0.1	0.1	0.1	0.1						
		3.0		0.36	0.50	0.44	0.44	V	* $V_{IN} = V_{IL}$ or V_{IH} 12 mA I_{OL} 24 mA 24 mA				
		4.5		0.36	0.50	0.44	0.44						
		5.5		0.36	0.50	0.44	0.44						
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	± 1.0	μA	$V_I = V_{CC}, \text{GND}$					

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74AC		54AC	74AC	Units	Conditions
			T _A = +25°C		T _A = -55°C to +125°C	T _A = -40°C to +85°C		
			Typ	Guaranteed Limits				
I _{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			-50	-75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V _{CC} (V)	74ACT		54ACT	74ACT	Units	Conditions	
			T _A = +25°C		T _A = -55°C to +125°C	T _A = -40°C to +85°C			
			Typ	Guaranteed Limits					
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
		5.5	1.5	2.0	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
		5.5	1.5	0.8	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I _{OUT} = -50 μA	
		5.5	5.49	5.4	5.4	5.4			
			4.5		3.86	3.70	3.76	V	*V _{IN} = V _{IL} or V _{IH} -24 mA I _{OH} = -24 mA
			5.5		4.86	4.70	4.76		
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1	0.1			
			4.5		0.36	0.50	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} = 24 mA
			5.5		0.36	0.50	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V _I = V _{CC} , GND	
I _{CC} T	Maximum I _{CC} /Input	5.5	0.6		1.6	1.5	mA	V _I = V _{CC} - 2.1V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V _{OLD} = 1.65V Max	
I _{OHD}		5.5			-50	-75	mA	V _{OHD} = 3.85V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V _{CC} * (V)	74AC			54AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	90 140	125 175		75 95		75 125	MHz		
t _{PLH}	Propagation Delay CP to Q _n	3.3 5.0	3.0 2.0	8.0 6.0	13.0 9.0	1.0 1.0	14.0 10.0	1.5 1.5	14.0 10.0	ns	2-3, 4
t _{PHL}	Propagation Delay CP to Q _n	3.3 5.0	3.5 2.5	8.5 6.5	13.0 10.0	1.0 1.0	15.0 11.0	2.0 1.5	14.5 11.0	ns	2-3, 4

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V _{CC} * (V)	74AC		54AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum						
t _s	Setup Time, HIGH or LOW D _n to CP	3.3 5.0	3.5 2.5	5.5 4.0		7.5 6.0		6.0 4.5	ns	2-7
t _h	Hold Time, HIGH or LOW D _n to CP	3.3 5.0	-2.0 -1.0	0 1.0		1.5 2.5		0 1.0	ns	2-7
t _s	Setup Time, HIGH or LOW CE to CP	3.3 5.0	4.0 2.5	6.0 4.0		9.5 6.0		7.5 4.5	ns	2-7
t _h	Hold Time, HIGH or LOW CE to CP	3.3 5.0	-3.5 -2.0	0 1.0		1.0 2.0		0 1.0	ns	2-7
t _w	CP Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5	5.5 4.0		6.5 5.0		6.0 4.5	ns	2-3

*Voltage Range 3.3 is 3.0V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V _{CC} * (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0	140	175		85		125	MHz		
t _{PLH}	Propagation Delay CP to Q _n	5.0	3.0	6.5	9.0	1.0	11.0	2.5	10.0	ns	2-3, 4
t _{PHL}	Propagation Delay CP to Q _n	5.0	3.5	7.0	10.0	1.0	12.0	2.5	11.0	ns	2-3, 4

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V _{CC} * (V)	74ACT		54ACT	74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -55°C to +125°C C _L = 50 pF	T _A = -40°C to +85°C C _L = 50 pF			
			Typ		Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to CP	5.0	2.5	4.5	7.0		5.5	ns	2-7
t _h	Hold Time, HIGH or LOW D _n to CP	5.0	-1.0	1.0	1.0		1.0	ns	2-7
t _s	Setup Time, HIGH or LOW CE to CP	5.0	2.5	4.5	7.0		5.5	ns	2-7
t _h	Hold Time, HIGH or LOW CE to CP	5.0	-1.0	1.0	1.0		1.0	ns	2-7
t _w	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	5.5		4.5	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0V
C _{PD}	Power Dissipation Capacitance	90.0	pF	V _{CC} = 5.0V