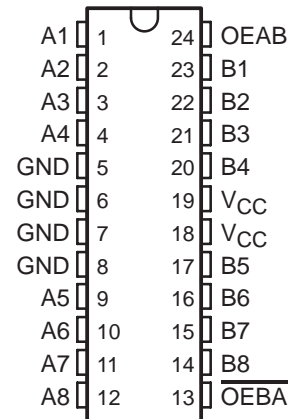


74AC11623
OCTAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCAS058A – JULY 1987 – REVISED APRIL 1993

- Local Bus-Latch Capability
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages, and Standard Plastic 300-mil DIPs

DW OR NT PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the output-enable (\overline{OEBA} or OEAB) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of OEAB and \overline{OEBA} . Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be complementary for the 74AC11623.

The 74AC11623 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS		OPERATION
\overline{OEBA}	OEAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

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recommended operating conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1		V
		V _{CC} = 4.5 V	3.15		
		V _{CC} = 5.5 V	3.85		
V _{IL}	Low-level input voltage	V _{CC} = 3 V	0.9		V
		V _{CC} = 4.5 V	1.35		
		V _{CC} = 5.5 V	1.65		
V _I	Input voltage	0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		V
I _{OH}	High-level output current	V _{CC} = 3 V	-4		mA
		V _{CC} = 4.5 V	-24		
		V _{CC} = 5.5 V	-24		
I _{OL}	Low-level output current	V _{CC} = 3 V	12		mA
		V _{CC} = 4.5 V	24		
		V _{CC} = 5.5 V	24		
Δt/Δv	Input transition rise or fall rate	0	10		ns/V
T _A	Operating free-air temperature	-40	85		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = - 50 μA	3 V	2.9		2.9		V	
		4.5 V	4.4		4.4			
		5.5 V	5.4		5.4			
	I _{OH} = - 4 mA	3 V	2.58		2.48			
		4.5 V	3.94		3.8			
		5.5 V	4.94		4.8			
I _{OH} = - 75 mA†	5.5 V			3.85				
V _{OL}	I _{OL} = 50 μA	3 V			0.1		V	
		4.5 V			0.1			
		5.5 V			0.1			
	I _{OL} = 12 mA	3 V			0.36			
		4.5 V			0.36			
		5.5 V			0.36			
I _{OL} = 75 mA†	5.5 V			1.65				
I _I	OEBA or OEAB	V _I = V _{CC} or GND	5.5 V	±0.1		±1		μA
I _{OZ} ‡	A or B ports	V _O = V _{CC} or GND	5.5 V	±0.5		±5		μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V	8		80		μA
C _i	OEBA or OEAB	V _I = V _{CC} or GND	5 V	4				pF
C _{io}	A or B ports	V _O = V _{CC} or GND	5 V	12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	1.5	6.8	9.2	1.5	10.5	ns
t_{PHL}			1.5	6.3	8.2	1.5	9.3	
t_{PZH}	$\overline{\text{OEBA}}$	A	1.5	8	10.6	1.5	12.2	ns
t_{PZL}			1.5	7.9	10.4	1.5	11.6	
t_{PHZ}	$\overline{\text{OEBA}}$	A	1.5	7	8.7	1.5	9.3	ns
t_{PLZ}			1.5	8	9.9	1.5	10.7	
t_{PZH}	OEAB	B	1.5	8.2	10.4	1.5	12	ns
t_{PZL}			1.5	8.3	10.8	1.5	12.2	
t_{PHZ}	OEAB	B	1.5	7	8.8	1.5	9.4	ns
t_{PLZ}			1.5	8	9.9	1.5	10.6	

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

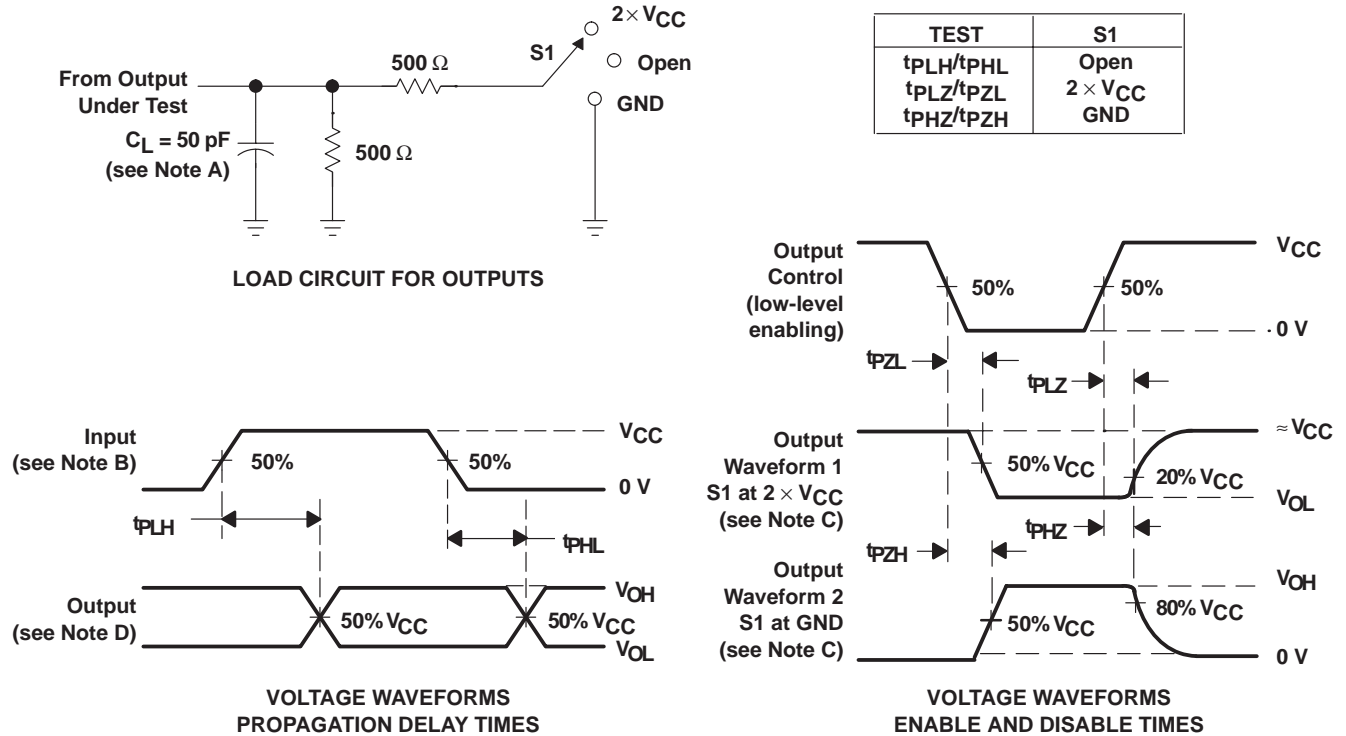
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	1.5	4.9	6.8	1.5	7.8	ns
t_{PHL}			1.5	4.6	6.4	1.5	7.1	
t_{PZH}	$\overline{\text{OEBA}}$	A	1.5	5.8	7.9	1.5	9	ns
t_{PZL}			1.5	5.9	8.1	1.5	9.1	
t_{PHZ}	$\overline{\text{OEBA}}$	A	1.5	6.1	7.7	1.5	8.3	ns
t_{PLZ}			1.5	6.6	8.2	1.5	8.8	
t_{PZH}	OEAB	B	1.5	6.2	8	1.5	9.2	ns
t_{PZL}			1.5	6.1	8.3	1.5	9.4	
t_{PHZ}	OEAB	B	1.5	6.2	7.8	1.5	8.3	ns
t_{PLZ}			1.5	6.5	8.1	1.5	8.8	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	49	pF
		Outputs disabled	9	



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$. For testing pulse duration: $t_r = t_f = 1 \text{ to } 3 \text{ ns}$. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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