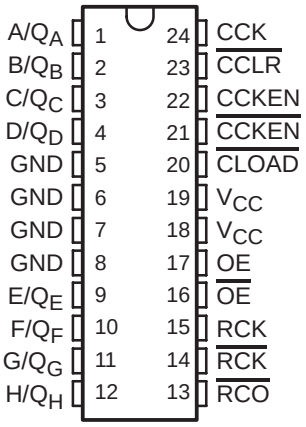
- **Parallel 3-State I/O: Register Inputs/ Counter Outputs**
- **Counter Has Direct Overriding Load and Clear**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

The 74AC11953 consists of a parallel input, an 8-bit storage register feeding an 8-bit counter, and a 3-state I/O which provides parallel count outputs. Both the register and the counter have individual positive-edge triggered clocks.

The function tables show the operation of the counter clock-enable (CCKEN, $\overline{\text{CCKEN}}$) and output-enable (OE, $\overline{\text{OE}}$) inputs. A register clock-enable ($\overline{\text{RCK}}$) input is also provided.

The counter ($\overline{\text{RCO}}$) input has direct load and clear functions. A low-going $\overline{\text{RCO}}$ pulse will be obtained when the counter reaches the hex word FF. Expansion is easily accomplished for two stages by connecting $\overline{\text{RCO}}$ of the first stage to $\overline{\text{CCKEN}}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{\text{RCO}}$ of each stage to CCK of the following stage.

The 74AC11593 is characterized for operation from − 40°C to 85°C.

Function Tables

COUNTER CLOCK ENABLE

INPUTS		OUTPUTS
CCKEN	$\overline{\text{CCKEN}}$	A/Q_A THRU H/Q_H
L	L	Enable
L	H	Disable
H	L	Enable
H	H	Enable

OUTPUT ENABLE

INPUTS		OUTPUTS
OE	$\overline{\text{OE}}$	A/Q_A THRU H/Q_H
L	L	Input mode
L	H	Input mode
H	L	Output mode
H	H	Input mode

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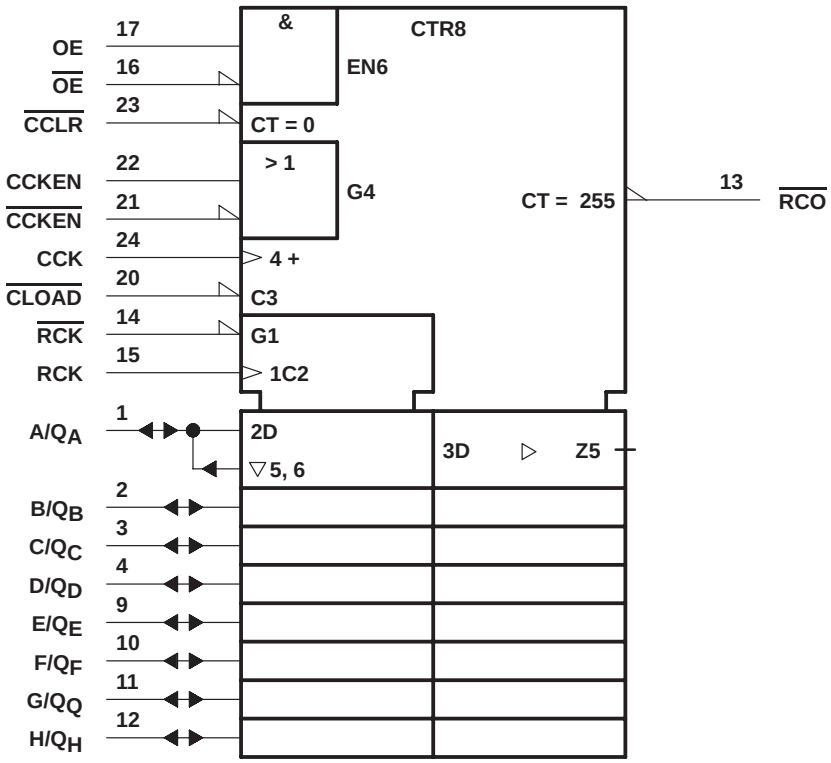
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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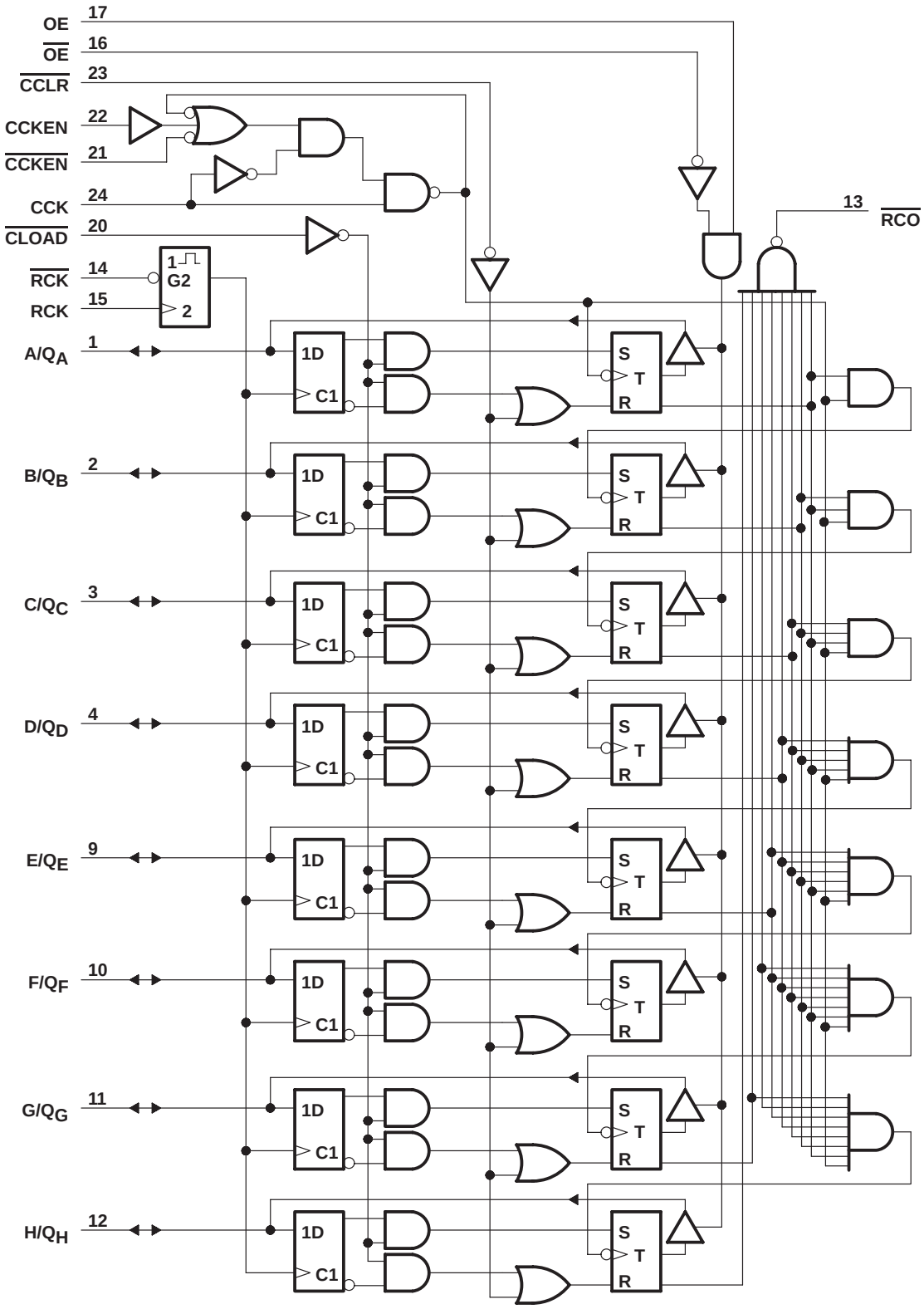
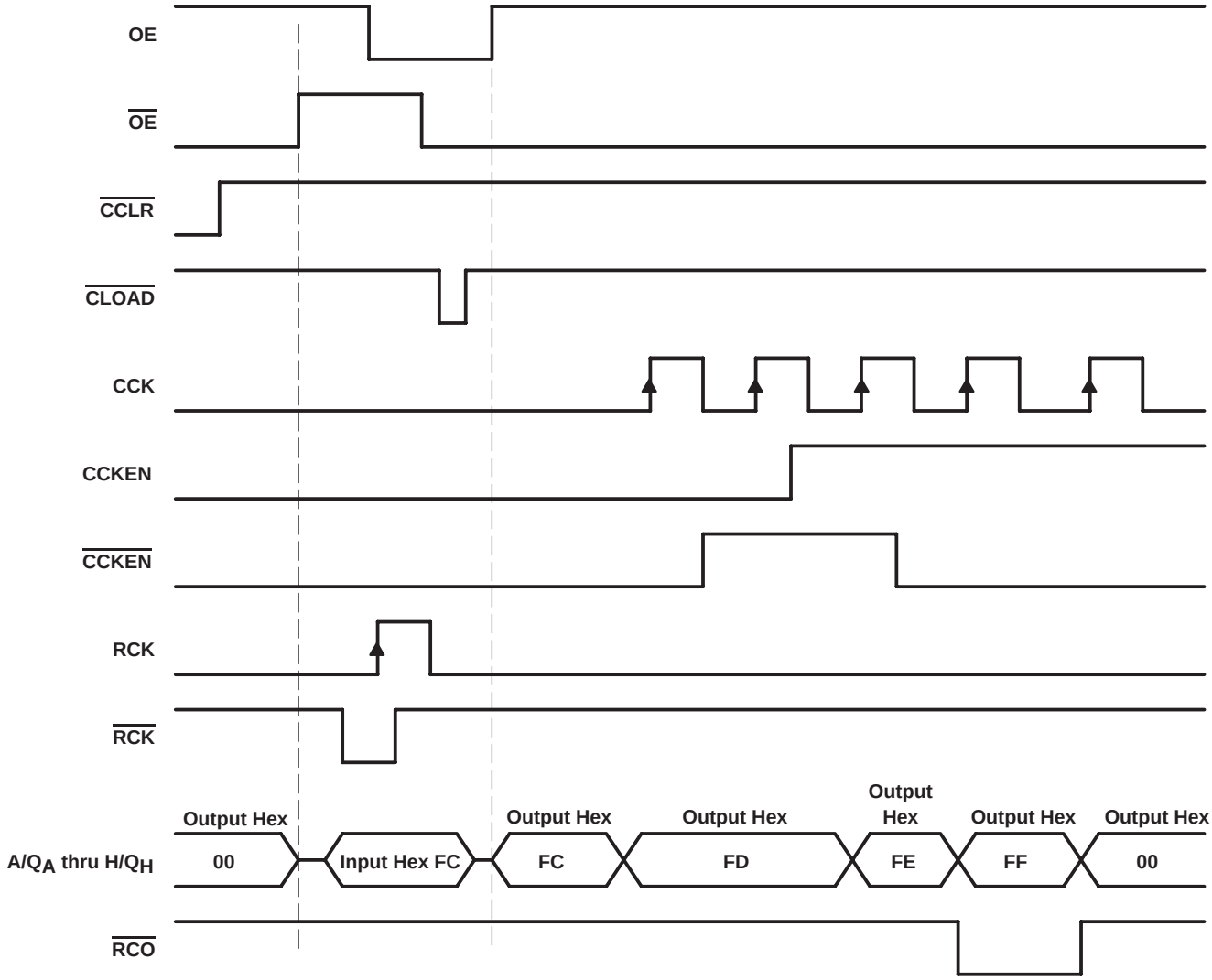
logic diagram (positive logic)



typical operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ± 50 mA
Continuous current through V_{CC} or GND . . . . . ± 225 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			− 4	mA
		V_{CC} = 4.5 V			− 24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		− 40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = − 50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = − 4 mA	3 V	2.58			2.48		
	I_{OH} = − 24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = − 75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			± 0.5		± 5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		4.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency, CCK or RCK			40		40	MHz
t_w	Pulse duration	CCK high or low	6		6		ns
		RCK high or low	6		6		
		$\overline{\text{RCK}}$ high or low	4.5		4.5		
		$\overline{\text{CCLR}}$ low	7.5		7.5		
		$\overline{\text{CLOAD}}$ low	6.1		6.1		
t_{su}	Setup time	$\overline{\text{CCKEN}}$ low before CCK↑	5.2		5.2		ns
		CCKEN high before CCK↑	6.4		6.4		
		$\overline{\text{CCLR}}$ high before CCK↑	1.7		1.7		
		$\overline{\text{CLOAD}}$ high before CCK↑	8.2		8.2		
		RCK↑ before $\overline{\text{CLOAD}}$↑†	11.1		11.1		
		Data A thru H before RCK↑	2.3		2.3		
t_h	Hold time	Data A thru H after RCK↑	0.5		0.5		ns
		All others	0.2		0.2		

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency, CCK or RCK			70		70	MHz
t_w	Pulse duration	CCK high or low	5		5		ns
		RCK high or low	5		5		
		$\overline{\text{RCK}}$ high or low	4.5		4.5		
		$\overline{\text{CCLR}}$ low	5		5		
		$\overline{\text{CLOAD}}$ low	4.7		4.7		
t_{su}	Setup time	$\overline{\text{CCKEN}}$ low before CCK↑	3.1		3.1		ns
		CCKEN high before CCK↑	4.3		4.3		
		$\overline{\text{CCLR}}$ high before CCK↑	1.1		1.1		
		$\overline{\text{CLOAD}}$ high before CCK↑	5.4		5.4		
		RCK↑ before $\overline{\text{CLOAD}}$↑†	7.8		7.8		
		Data A thru H before RCK↑	2		2		
t_h	Hold time	Data A thru H after RCK↑	1.1		1.1		ns
		All others	0.8		0.8		

† This time insures the data saved by RCK↑ will also be loaded into the counter.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			40			40		MHz
t_{PLH}	CCK	Q	6.8	14.4	19.3	6.8	22.4	ns
t_{PHL}			6.4	14.1	18.8	6.4	21.1	
t_{PLH}	$\overline{CLOAD}$	Q	6.7	17.3	23.6	6.7	27.1	ns
t_{PHL}			3.9	18.9	29.1	3.9	32.3	
t_{PHL}	$\overline{CCLR}$	Q	5.4	13	17.6	5.4	19.8	ns
t_{PZH}	OE	Q	7.3	15.7	20.8	7.3	24.1	ns
t_{PZL}			8	17.7	23.2	8	26.7	
t_{PZH}	$\overline{OE}$	Q	6.9	15.2	20.2	6.9	23.3	ns
t_{PZL}			7.8	17.3	22.7	7.8	26.1	
t_{PHZ}	OE	Q	6.4	10.3	13.8	6.4	15.2	ns
t_{PLZ}			6.6	10.8	14.1	6.6	16.1	
t_{PHZ}	$\overline{OE}$	Q	5.7	9.6	12.8	5.7	14.1	ns
t_{PLZ}			5.9	10.2	13.4	5.9	15.2	
t_{PLH}	CCK	$\overline{RCO}$	5.3	12	16	5.3	18.6	ns
t_{PHL}			7.1	15.4	20.3	7.1	23.1	
t_{PLH}	$\overline{CLOAD}$	$\overline{RCO}$	5.9	12.4	16.5	5.9	18.8	ns
t_{PHL}			10.1	19.6	25.5	10.1	29.4	
t_{PLH}	$\overline{CCLR}$	$\overline{RCO}$	5.6	12.3	16.6	5.6	19.2	ns
t_{PLH}	RCK	$\overline{RCO}$	8.6	17.3	22.2	8.6	25.8	ns
t_{PHL}			10.3	20.3	26.2	10.3	30.3	

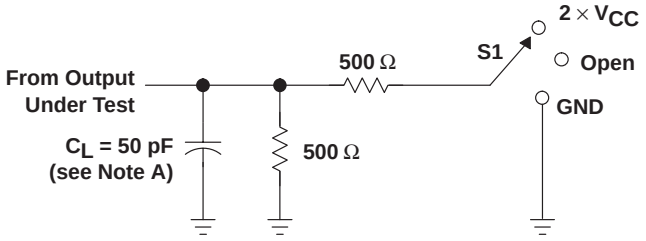
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			70			70		MHz
t_{PLH}	CCK	Q	4.1	8.7	12.4	4.1	14.3	ns
t_{PHL}			4.2	8.9	12.6	4.2	14.2	
t_{PLH}	$\overline{CLOAD}$	Q	3.7	10	15.3	3.7	17.4	ns
t_{PHL}			3.4	11.4	18.3	3.4	20.6	
t_{PHL}	$\overline{CCLR}$	Q	3.3	7.9	11.8	3.3	13.4	ns
t_{PZH}	OE	Q	4.1	9.1	13.2	4.1	15.3	ns
t_{PZL}			4.1	9.4	13.8	4.1	16	
t_{PZH}	$\overline{OE}$	Q	3.8	8.7	13	3.8	15	ns
t_{PZL}			3.9	9.1	13.4	3.9	15.4	
t_{PHZ}	OE	Q	4.2	7.6	10.6	4.2	11.6	ns
t_{PLZ}			5.3	8.8	11.8	5.3	13.1	
t_{PHZ}	$\overline{OE}$	Q	4.4	7.3	10.1	4.4	11	ns
t_{PLZ}			5.2	8.5	11.6	5.2	13	
t_{PLH}	CCK	$\overline{RCO}$	3.5	7.6	11.2	3.5	12.8	ns
t_{PHL}			4.1	9.2	13.4	4.1	15.4	
t_{PLH}	$\overline{CLOAD}$	$\overline{RCO}$	3.5	7.8	11.2	3.5	12.8	ns
t_{PHL}			5.6	11.7	16.6	5.6	19	
t_{PLH}	$\overline{CCLR}$	$\overline{RCO}$	3.6	8	11.6	3.6	13.4	ns
t_{PLH}	RCK	$\overline{RCO}$	5	10.3	14.4	5	16.7	ns
t_{PHL}			5.5	11.7	16.6	5.5	19.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

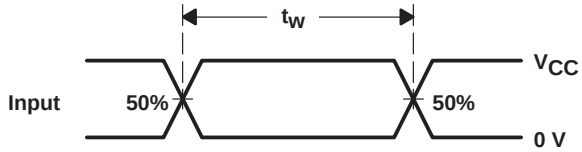
PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF,	f = 1 MHz	66	pF
		Outputs disabled			15	

PARAMETER MEASUREMENT INFORMATION

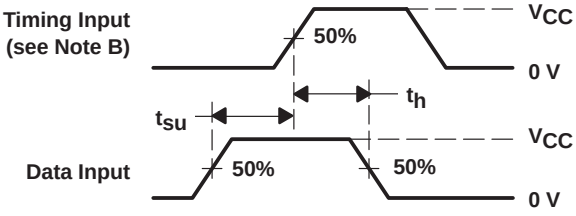


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

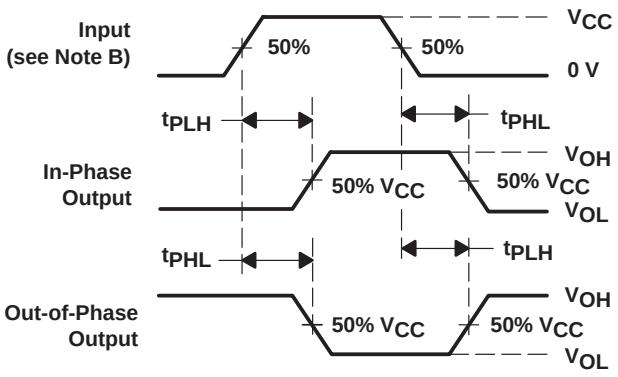
LOAD CIRCUIT



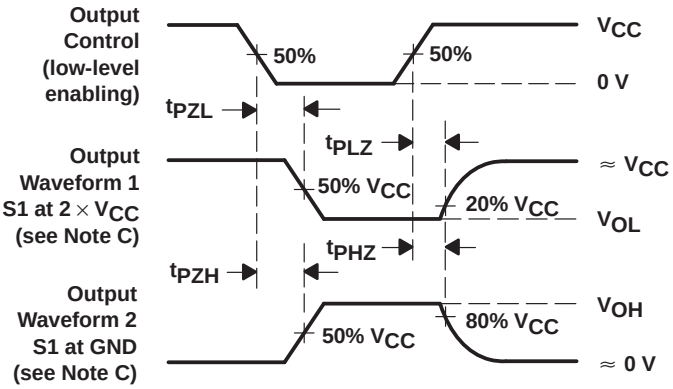
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74AC11593DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
74AC11593DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
74AC11593DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
74AC11593NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
74AC11593NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265