

# 54/7473 54H/74H73 54LS/74LS73

## DUAL JK FLIP-FLOP

(With Separate Clears and Clocks)

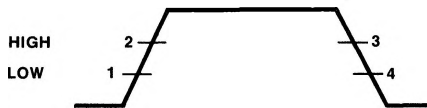
**DESCRIPTION** — The '73 and 'H73 dual JK master/slave flip-flops have a separate clock for each flip-flop. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) isolate slave from master; 2) enter information from J and K inputs to master; 3) disable J and K inputs; 4) transfer information from master to slave.

**TRUTH TABLE**

| INPUTS  |   | OUTPUT      |
|---------|---|-------------|
| @ $t_n$ |   | @ $t_{n+1}$ |
| J       | K | Q           |
| L       | L | $Q_n$       |
| L       | H | L           |
| H       | L | H           |
| H       | H | $\bar{Q}_n$ |

H = HIGH Voltage Level  
L = LOW Voltage Level  
 $t_n$  = Bit time before clock pulse.  
 $t_{n+1}$  = Bit time after clock pulse.

**CLOCK WAVEFORM**



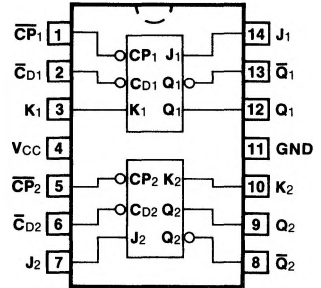
Asynchronous Input:  
LOW input to  $\bar{C}_D$  sets Q to LOW level  
Clear is independent of clock

The 'LS73 offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

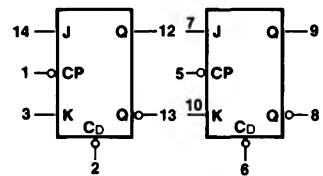
**ORDERING CODE:** See Section 9

| PKGS            | PIN OUT | COMMERCIAL GRADE  | MILITARY GRADE  | PKG TYPE |
|-----------------|---------|---|---|----------|
|                 |         | $V_{CC} = +5.0\text{ V} \pm 5\%$ ,<br>$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ | $V_{CC} = +5.0\text{ V} \pm 10\%$ ,<br>$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ |          |
| Plastic DIP (P) | A       | 7473PC, 74H73PC<br>74LS73PC   |   | 9A       |
| Ceramic DIP (D) | A       | 7473DC, 74H73DC<br>74LS73DC   | 5473DM, 54H73DM<br>54LS73DM   | 6A       |
| Flatpak (F)     | A       | 7473FC, 74H73FC<br>74LS73FC   | 5473FM, 54H73FM<br>54LS73FM   | 3I       |

**CONNECTION DIAGRAM  
PINOUT A**



**LOGIC SYMBOL**

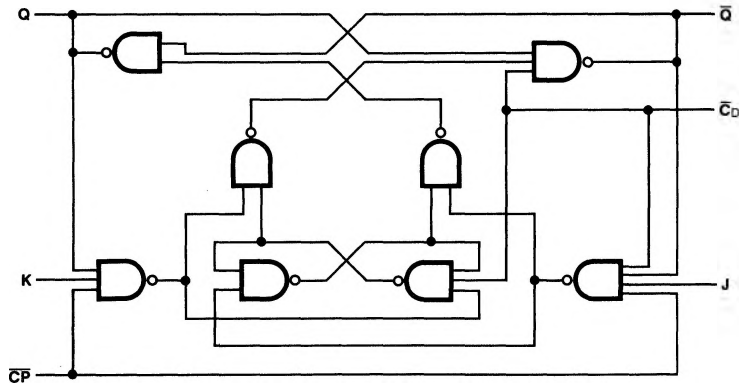


$V_{CC}$  = Pin 4  
GND = Pin 11

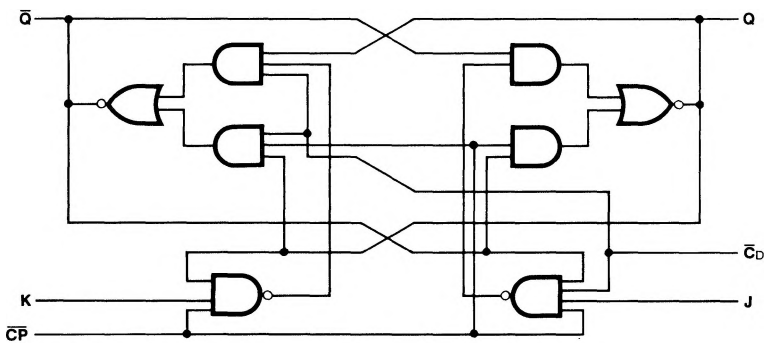
**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PIN NAMES   | DESCRIPTION                              | 54/74 (U.L.)<br>HIGH/LOW | 54/74H (U.L.)<br>HIGH/LOW | 54/74LS (U.L.)<br>HIGH/LOW |
|---|--|--------------------------|---------------------------|----------------------------|
| J <sub>1</sub> , J <sub>2</sub> , K <sub>1</sub> , K <sub>2</sub>   | Data Inputs                              | 1.0/1.0                  | 1.25/1.25                 | 0.5/0.25                   |
| CP <sub>1</sub> , CP <sub>2</sub>                                   | Clock Pulse Inputs (Active Falling Edge) | 2.0/2.0                  | 1.25/1.25                 | 2.0/0.5                    |
| CD <sub>1</sub> , CD <sub>2</sub>                                   | Direct Clear Inputs (Active LOW)         | 2.0/2.0                  | 2.5/2.5                   | 1.5/0.5                    |
| Q <sub>1</sub> , Q <sub>2</sub> , Q̄ <sub>1</sub> , Q̄ <sub>2</sub> | Outputs                                  | 20/10                    | 12.5/12.5                 | 10/5.0<br>(2.5)            |

**LOGIC DIAGRAMS** (one half shown)  
'73, 'H73



'LS73



**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| SYMBOL          | PARAMETER            | 54/74 |     | 54/74H |     | 54/74LS |     | UNITS | CONDITIONS                                      |
|-----------------|----------------------|-------|-----|--------|-----|---------|-----|-------|---|
|                 |                      | Min   | Max | Min    | Max | Min     | Max |       |   |
| I <sub>CC</sub> | Power Supply Current | 40    |     | 50     |     | 8.0     |     | mA    | V <sub>CC</sub> = Max,<br>V <sub>CP</sub> = 0 V |

**AC CHARACTERISTICS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C (See Section 3 for waveforms and load configurations)

| SYMBOL                               | PARAMETER                                       | 54/74  |     | 54/74H   |     | 54/74LS                |     | UNITS | CONDITIONS      |
|--------------------------------------|---|--|-----|--|-----|------------------------|-----|-------|-----------------|
|                                      |   | C <sub>L</sub> = 15 pF<br>R <sub>L</sub> = 400 Ω |     | C <sub>L</sub> = 25 pF<br>R <sub>L</sub> = 280 Ω |     | C <sub>L</sub> = 15 pF |     |       |                 |
|                                      |   | Min  | Max | Min  | Max | Min                    | Max |       |                 |
| f <sub>max</sub>                     | Maximum Clock Frequency                         | 15   |     | 25   |     | 30                     |     | MHz   | Fig. 3-1, 3-9   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>C <sub>Pn</sub> to Q or Q̄ | 25<br>40   |     | 21<br>27   |     | 20<br>30               |     | ns    | Figs. 3-1, 3-9  |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>C <sub>Dn</sub> to Q or Q̄ | 25<br>40   |     | 13<br>24   |     | 20<br>30               |     | ns    | Figs. 3-1, 3-10 |

**AC OPERATING REQUIREMENTS:** V<sub>CC</sub> = +5.0 V T<sub>A</sub> = +25°C

| SYMBOL                                   | PARAMETER  | 54/74    |     | 54/74H   |     | 54/74LS    |     | UNITS | CONDITIONS                                    |
|--|--|----------|-----|----------|-----|------------|-----|-------|---|
|  |  | Min      | Max | Min      | Max | Min        | Max |       |   |
| t <sub>s</sub> (H)                       | Setup Time HIGH<br>J <sub>n</sub> or K <sub>n</sub> to C <sub>Pn</sub> | 0        |     | 0        |     | 20         |     | ns    | Fig. 3-18<br>( '73, 'H73)<br>Fig. 3-7 ('LS73) |
| t <sub>h</sub> (H)                       | Hold Time HIGH<br>J <sub>n</sub> or K <sub>n</sub> to C <sub>Pn</sub>  | 0        |     | 0        |     | 0          |     | ns    |   |
| t <sub>s</sub> (L)                       | Setup Time LOW<br>J <sub>n</sub> or K <sub>n</sub> to C <sub>Pn</sub>  | 0        |     | 0        |     | 20         |     | ns    |   |
| t <sub>h</sub> (L)                       | Hold Time LOW<br>J <sub>n</sub> or K <sub>n</sub> to C <sub>Pn</sub>   | 0        |     | 0        |     | 0          |     | ns    |   |
| t <sub>w</sub> (H)<br>t <sub>w</sub> (L) | C <sub>Pn</sub> Pulse Width  | 20<br>47 |     | 12<br>16 |     | 13.5<br>20 |     | ns    | Fig. 3-9                                      |
| t <sub>w</sub> (L)                       | C <sub>Dn</sub> Pulse Width LOW  | 25       |     | 16       |     | 25         |     | ns    | Figs. 3-1, 3-10                               |