

# 54/7446A • 54/7447A 54LS/74LS47

## BCD TO 7-SEGMENT DECODER/DRIVER

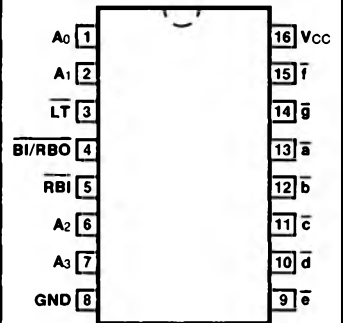
**DESCRIPTION** — The '46A, '47A and 'LS47 accept four lines of BCD (8421) input data, generate their complements internally and decode the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 40 mA (24 mA for the 'LS47) in the ON (LOW) state and withstand 15 V (30 V for the '46A) in the OFF (HIGH) state with a maximum leakage current of 250  $\mu$ A. Auxiliary inputs provide blanking, lamp test and cascadable zero-suppression functions. Also see the 'LS247 data sheet.

- OPEN-COLLECTOR OUTPUTS
- DRIVE INDICATOR SEGMENTS DIRECTLY
- CASCADABLE ZERO-SUPPRESSION CAPABILITY
- LAMP TEST INPUT

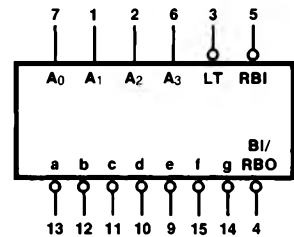
**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 V \pm 5\%$ , $T_A = 0^\circ C \text{ to } +70^\circ C$	$V_{CC} = +5.0 V \pm 10\%$ , $T_A = -55^\circ C \text{ to } +125^\circ C$	
Plastic DIP (P)	A	7446APC, 7447APC 74LS47PC		9B
Ceramic DIP (D)	A	7446ADC, 7447ADC 74LS47DC	5446ADM, 5447ADM 54LS47DM	7B
Flatpak (F)	A	7446AFC, 7447AFC 74LS47FC	5446AFM, 5447AFM 54LS47FM	4L

### CONNECTION DIAGRAM PINOUT A



### LOGIC SYMBOL



$V_{CC} = \text{Pin } 16$   
 $GND = \text{Pin } 8$

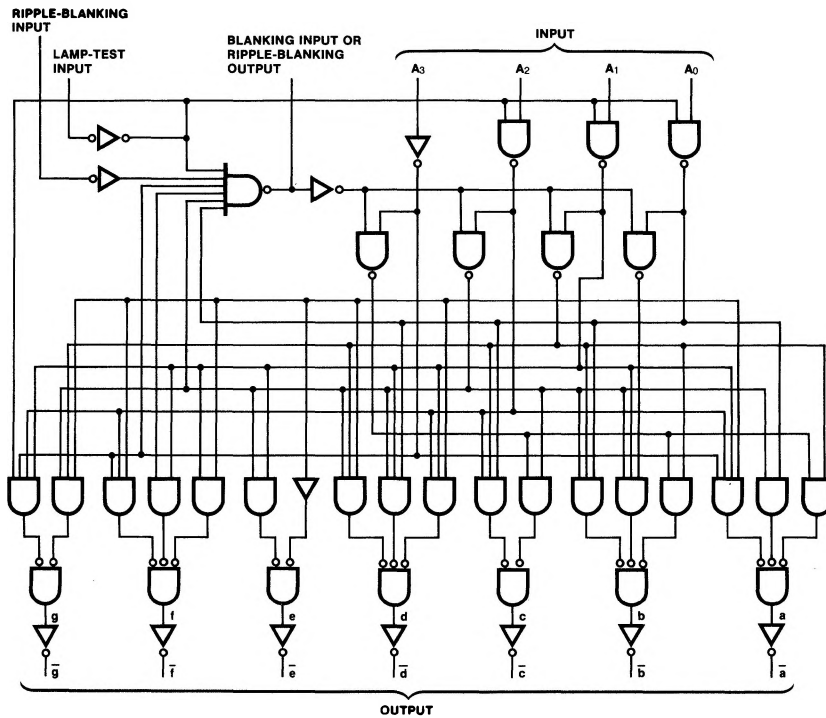
**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	BCD Inputs	1.0/1.0	0.5/0.25
RBI	Ripple Blanking Input (Active LOW)	1.0/1.0	0.5/0.25
LT	Lamp Test Input (Active LOW)	1.0/1.0	0.5/0.25
BI/RBO	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)	-/2.5 5.0/5.0	-/0.75 1.25/2.0
$\bar{a} - \bar{g}$	Segment Outputs (Active LOW)	OC*/25	(1.0) OC*/15 (7.5)

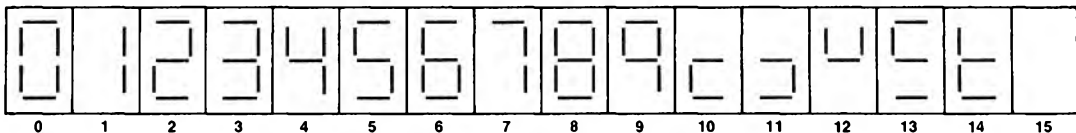
\*OC — Open Collector

**FUNCTIONAL DESCRIPTION** — The '46A, '47A and 'LS47 decode the input data in the pattern indicated in the Truth Table and the segment identification illustration. If the input data is decimal zero, a LOW signal applied to the  $\overline{\text{RBI}}$  blanks the display and causes a multidigit display. For example, by grounding the  $\overline{\text{RBI}}$  of the highest order decoder and connecting its  $\overline{\text{BI/RBO}}$  to  $\overline{\text{RBI}}$  of the next lowest order decoder, etc., leading zeros will be suppressed. Similarly, by grounding  $\overline{\text{RBI}}$  of the lowest order decoder and connecting its  $\overline{\text{BI/RBO}}$  to  $\overline{\text{RBI}}$  of the next highest order decoder, etc., trailing zeros will be suppressed. Leading and trailing zeros can be suppressed simultaneously by using external gates, i.e. by driving  $\overline{\text{RBI}}$  of an intermediate decoder from an OR gate whose inputs are  $\overline{\text{BI/RBO}}$  of the next highest and lowest order decoders.  $\overline{\text{BI/RBO}}$  also serves as an unconditional blanking input. The internal NAND gate that generates the  $\overline{\text{RBO}}$  signal has a resistive pull-up, as opposed to a totem pole, and thus  $\overline{\text{BI/RBO}}$  can be forced LOW by external means, using wired-collector logic. A LOW signal thus applied to  $\overline{\text{BI/RBO}}$  turns off all segment outputs. This blanking feature can be used to control display intensity by varying the duty cycle of the blanking signal. A LOW signal applied to LT turns on all segment outputs, provided that  $\overline{\text{BI/RBO}}$  is not forced LOW.

**LOGIC DIAGRAM**



**NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS**



TRUTH TABLE

DECIMAL OR FUNCTION	INPUTS						OUTPUTS							NOTE	
	$\overline{\text{LT}}$	$\overline{\text{RBI}}$	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	$\overline{\text{BI/RBO}}$	$\overline{\text{a}}$	$\overline{\text{b}}$	$\overline{\text{c}}$	$\overline{\text{d}}$	$\overline{\text{e}}$	$\overline{\text{f}}$		$\overline{\text{g}}$
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	1
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	1
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{\text{BI}}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	2
$\overline{\text{RBI}}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	3
$\overline{\text{LT}}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	4

NOTES:

- (1)  $\overline{\text{BI/RBO}}$  is wire-AND logic serving as blanking input ( $\overline{\text{BI}}$ ) and/or ripple-blanking output ( $\overline{\text{RBO}}$ ). The blanking out ( $\overline{\text{BI}}$ ) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ( $\overline{\text{RBI}}$ ) must be open or at a HIGH level if blanking or a decimal 0 is not desired. X = input may be HIGH or LOW.
- (2) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a HIGH level regardless of the state of any other input condition.
- (3) When ripple-blanking input ( $\overline{\text{RBI}}$ ) and inputs A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub> and A<sub>3</sub> are LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ( $\overline{\text{RBO}}$ ) goes to a LOW level (response condition).
- (4) When the blanking input/ripple-blanking output ( $\overline{\text{BI/RBO}}$ ) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

SYMBOL	PARAMETER		54/74		54/74LS		UNITS	CONDITIONS	
			Min	Max	Min	Max			
I <sub>OH</sub>	Output HIGH Current OFF State at $\bar{a}-\bar{g}$	'46	250				$\mu\text{A}$	$V_{OH} = 30\text{ V}$	$V_{CC} = \text{Max}$
		'47	250	250		$V_{OH} = 15\text{ V}$			
I <sub>OS</sub>	Output Short Circuit Current at $\overline{\text{BI/RBO}}$		-4.0	-0.3	-2.0		mA	$V_{CC} = \text{Max}$	
I <sub>CC</sub>	Power Supply Current	XM	85		13		mA	$V_{CC} = \text{Max}$	
		XC	103		13				

**AC CHARACTERISTICS:**  $V_{CC} = +5.0\text{ V}$ ,  $T_A = +25^\circ\text{C}$  (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER		54/74		54/74LS		UNITS	CONDITIONS	
			$C_L = 15\text{ pF}$ $R_L = 120\ \Omega$		$C_L = 15\text{ pF}$ $R_L = 665\ \Omega$				
			Min	Max	Min	Max			
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $A_n$ to $\bar{a}-\bar{g}$		100	100	100	100	ns	Figs. 3-2, 3-20	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\overline{\text{RBI}}$ to $\bar{a}-\bar{f}$		100	100	100	100	ns	Figs. 3-2, 3-4 LT = HIGH, $A_0 - A_3 = \text{LOW}$	