54/74191
54LS/74LS191

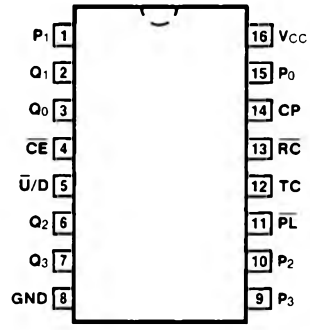
UP/DOWN BINARY COUNTER

(With Preset and Ripple Clock)

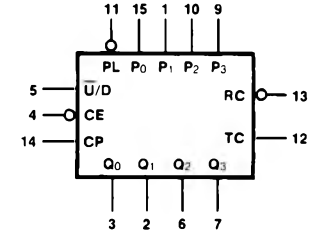
DESCRIPTION — The '191 is a reversible modulo-16 binary counter featuring synchronous counting and asychronous presetting. The preset feature allows the '191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multi-stage counters. In the counting modes, state changes are initiated by the rising edge of the clock. For detail specifications and functional description, please refer to the '190 data sheet.

- **HIGH SPEED — 30 MHz TYPICAL COUNT FREQUENCY**
- **SYNCHRONOUS COUNTING**
- **ASYNCHRONOUS PARALLEL LOAD**
- **CASCADABLE**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10% TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74191PC, 74LS191PC		9B
Ceramic DIP (D)	A	74191DC, 74LS191DC	54191DM, 54LS191DM	7B
Flatpak (F)	A	74191FC, 74LS191FC	54191FM, 54LS191FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CE}$	Count Enable Input (Active LOW)	3.0/3.0	1.5/0.75
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	0.5/0.25
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0	0.5/0.25
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{U}$/D	Up/Down Count Control Input	1.0/1.0	0.5/0.25
$Q_0 - Q_3$	Flip-flop Outputs	20/10	10/5.0 (2.5)
$\overline{RC}$	Ripple Clock Output (Active LOW)	20/10	10/5.0 (2.5)
TC	Terminal Count Output (Active HIGH)	20/10	10/5.0 (2.5)

MODE SELECT TABLE

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⌐	Count Up
H	L	H	⌐	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

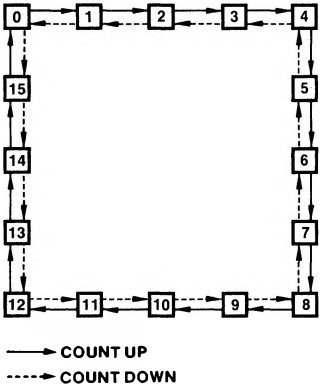
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

RC TRUTH TABLE

INPUTS			OUTPUT
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⌐	⌐
H	X	X	H
X	L	X	H

*TC is generated internally

STATE DIAGRAM



LOGIC DIAGRAM